

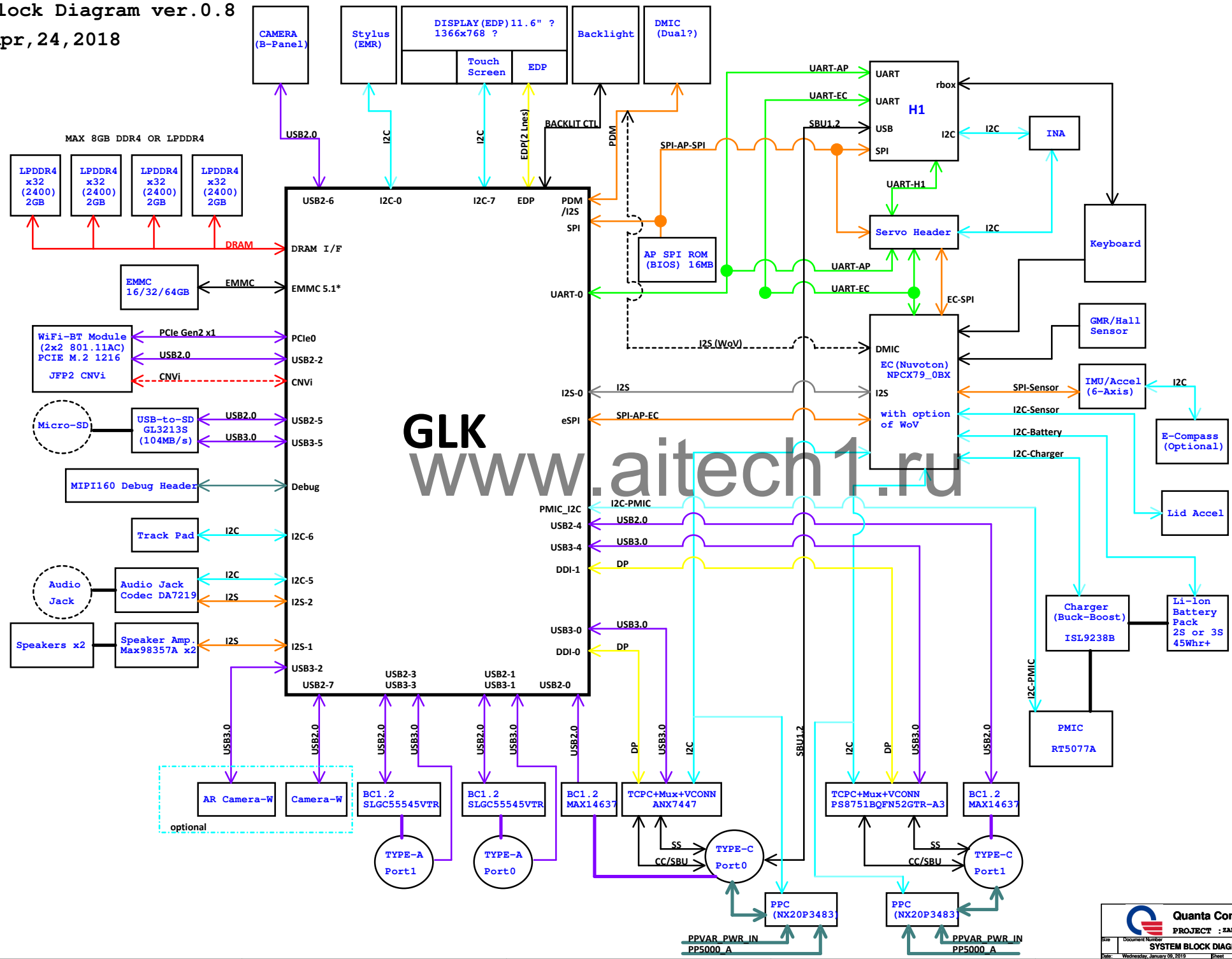
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ASSY:650-01771-03
PCB: 651-01771-03

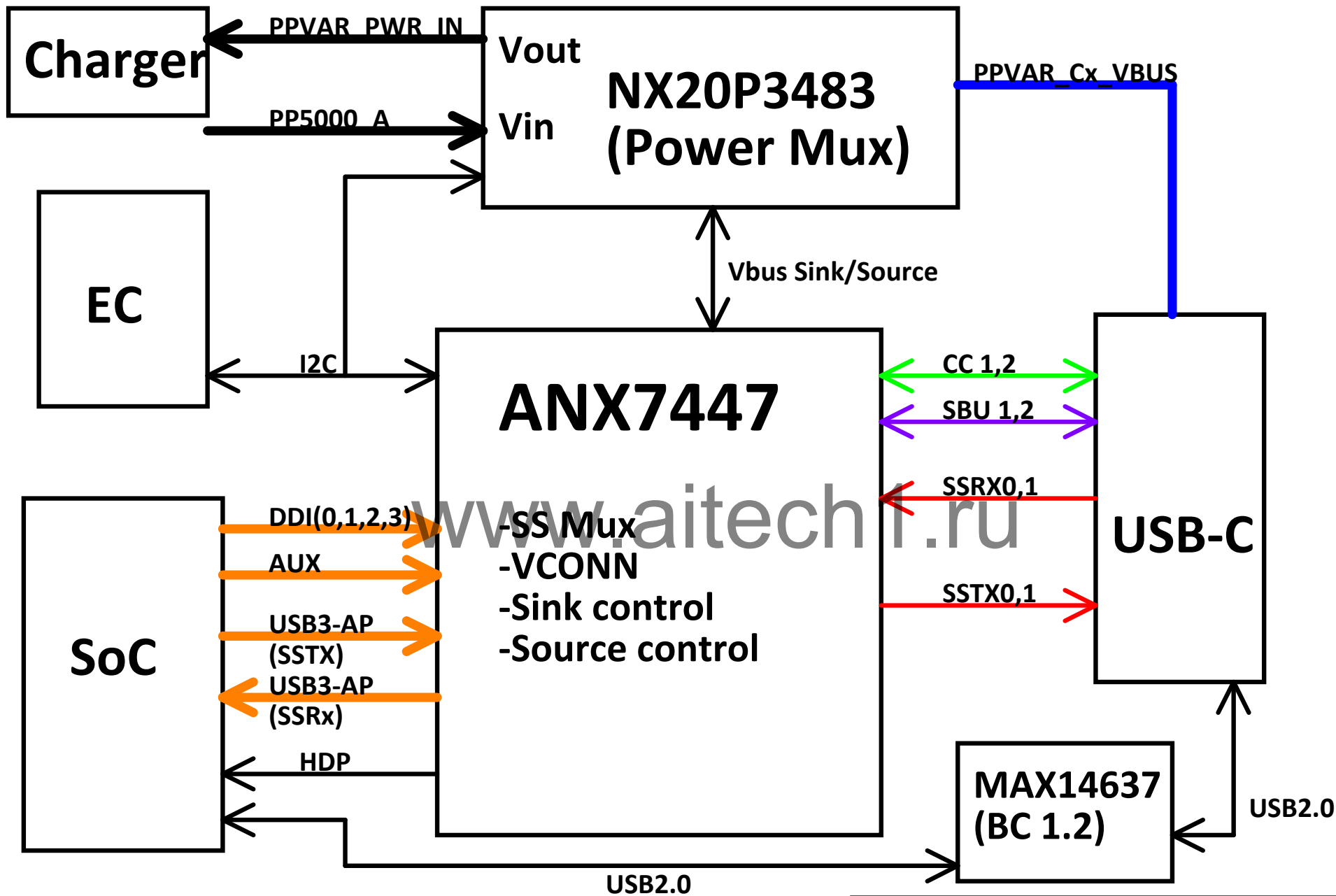
SHEET NO.	SHEET NAME
1	TABLE OF CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	USB TYPE-C BLOCK DIAGRAM
4	POWER TREE
5	I2C MAP
6	SOC DRAM I/F
7	SOC EDP/MIPI/DDI
8	SOC PCIE/USB/SATA
9	SOC AUDIO/EMMC/LPC/SPI
10	SOC I2C/CNVI/UART/SPI
11	SOC PMU/RTC/SVID/THERMAL/MISC
12	SOC JTAG/GPIO/ITP
13	SOC GROUND
14	SOC POWER
15	SOC DECOUPLING
16	MEMORY CH 00/01 LPDDR4
17	MEMORY CH 10/11 LPDDR4
18	EC-NUVOTON
19	SPI ROM
20	MIPI60 DEBUG HEADER
21	H1 SECURE MICROCONTROLLER
22	SERVO
23	eMMC/SD
24	AUDIO
25	KB, TP, PEN
26	LID: eDP, CAM, TOUCH, SENSOR
27	SENSOR: COMPASS, GYRO
28	WIFI/BT CONNECTOR
29	USB C TCPC/MUX
30	USB A CONNECTIONS (MLB)

[illegible]

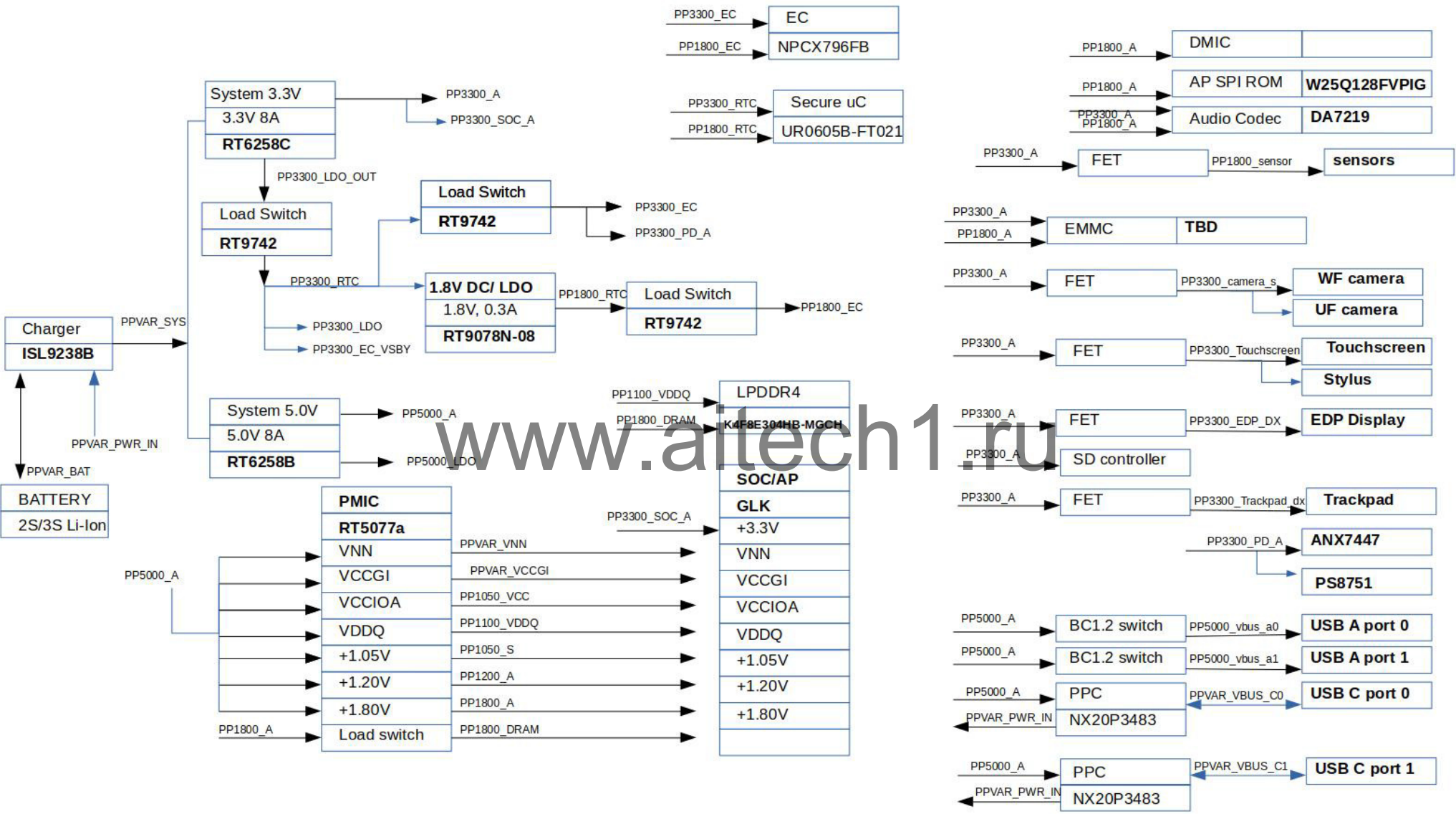
Octopus (Gemini Lake)
Block Diagram ver.0.8

Apr, 24, 2018

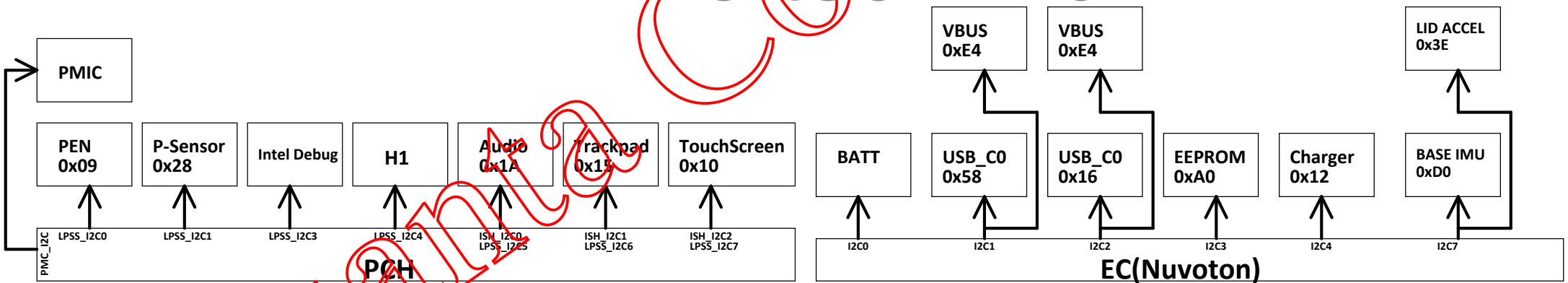


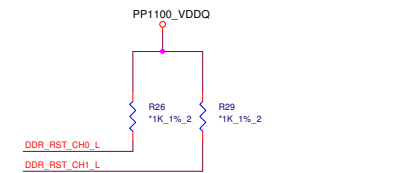


Power Tree



Master	Port	Net Name	Slave Device(S)	Speed
EC	I2C0 0	EC I2C BATTERY 3V3	BATTERY (TBD)	100KHZ
EC	I2C1 0	EC I2C USB C0 MUX	ANX7447, NX20P3483 <i>Check subboard</i>	100KHZ
EC	I2C2 0	EC I2C USB C1 MUX		100KHZ
EC	I2C3 0	EC I2C EEPROM SCL	M34E02	100KHZ
EC	I2C4 1	EC I2C CHARGER 3V3	ISL9238B	100KHZ
EC	I2C5 0	-		
EC	I2C7 0	EC I2C SENSOR U	LSM6DS3TR, LIS2MDLTR	400KHZ
AP	LPSS I2C0	PCH I2C PEN	STYLUS (TBD)	400KHZ
AP	LPSS I2C1	PCH I2C P SENSOR	TBD	100KHZ
AP	LPSS I2C2	-		
AP	LPSS I2C3	DBG PCH I2C	TBD	TBD
AP	LPSS I2C4	PCH I2C H1	H1 (not used)	100KHZ
AP	LPSS I2C5	PCH I2C AUDIO	DA7219	100KHZ
AP	LPSS I2C6	PCH I2C TRACKPAD	TRACKPAD (TBD)	100KHZ
AP	LPSS I2C7	PCH I2C TOUCHSCREEN	TOUCHSCREEN (TBD)	100KHZ
AP	PMC I2C	PCH PMIC I2C	RT5077A	100KHZ

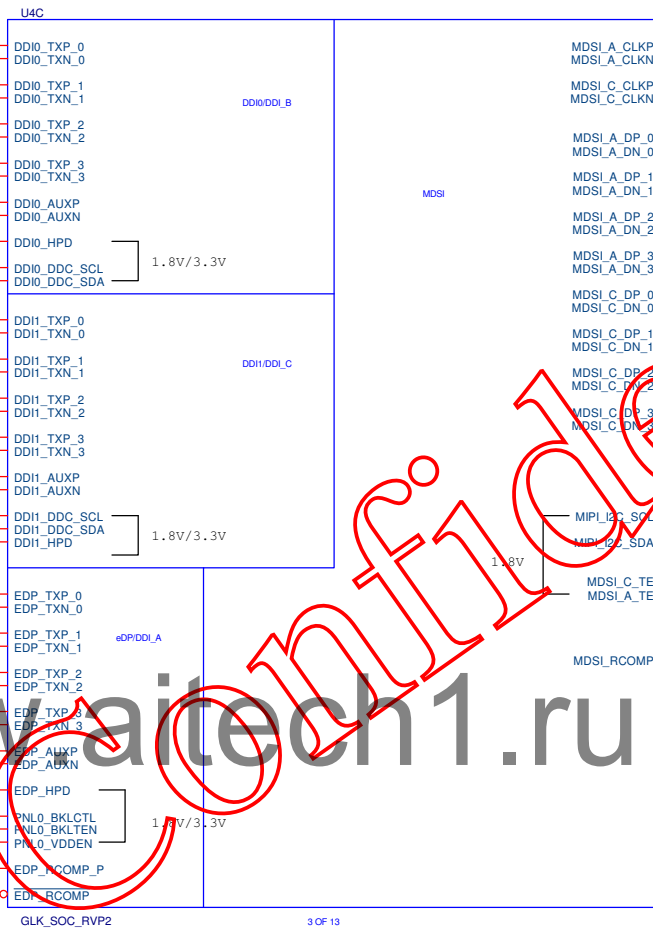
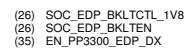


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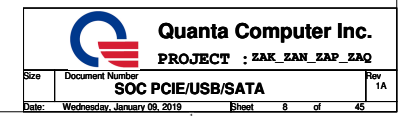
(CPU)



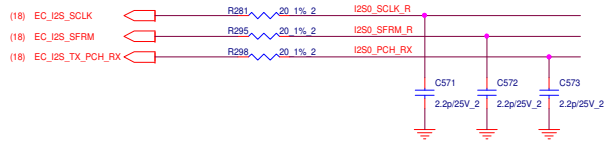
LOCAL DISPLAY PANEL



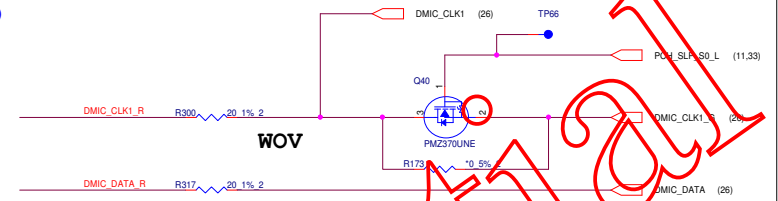
(CPU)



(CPU)



(MIC)



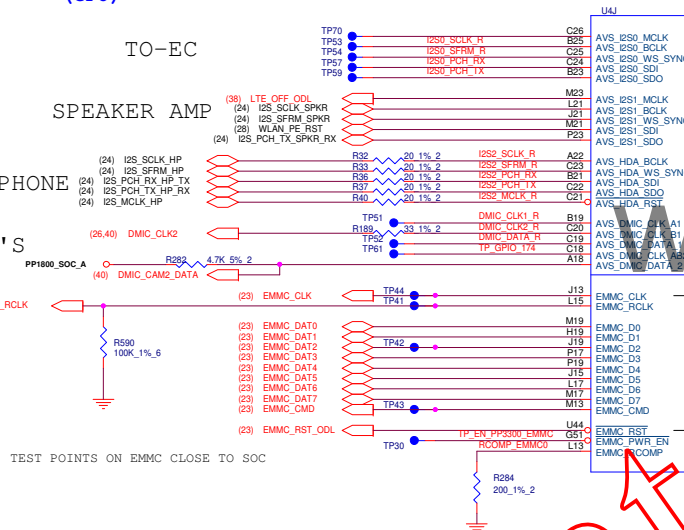
(CPU)

TO-EC

SPEAKER AMP

HEADPHONE

DMIC'S



TEST POINTS ON EMMC CLOSE TO SOC

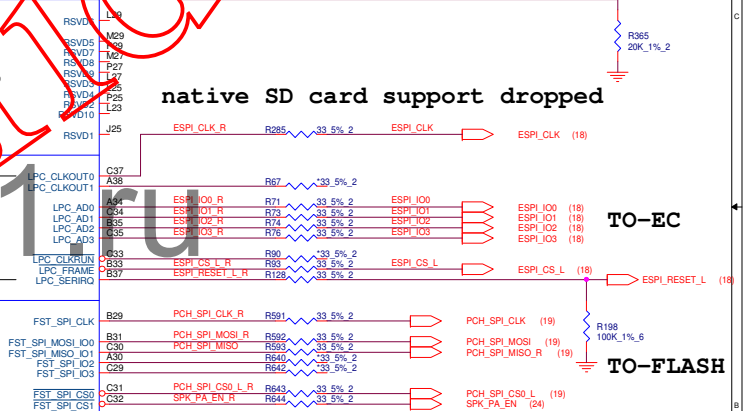
LPC set 3.3V

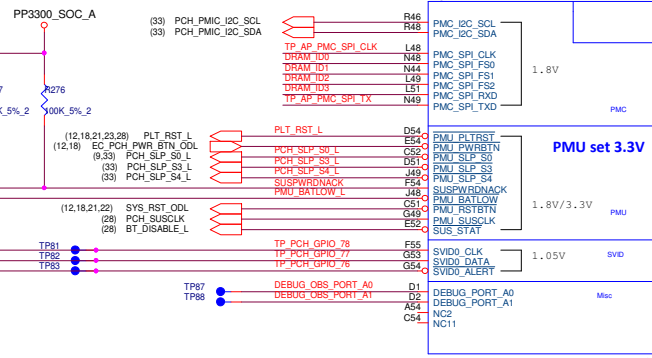
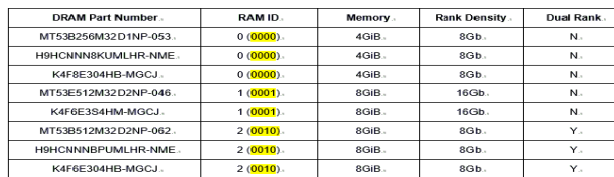
7 OF 12

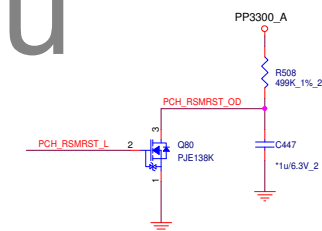
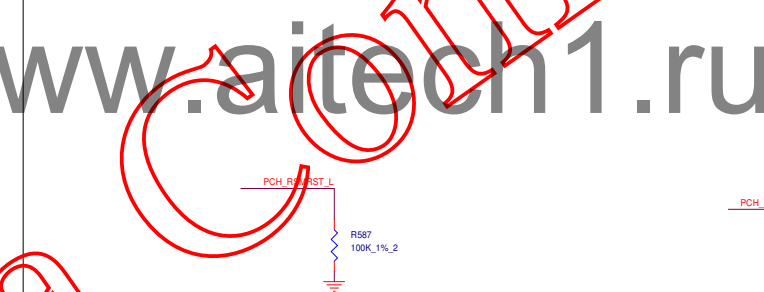
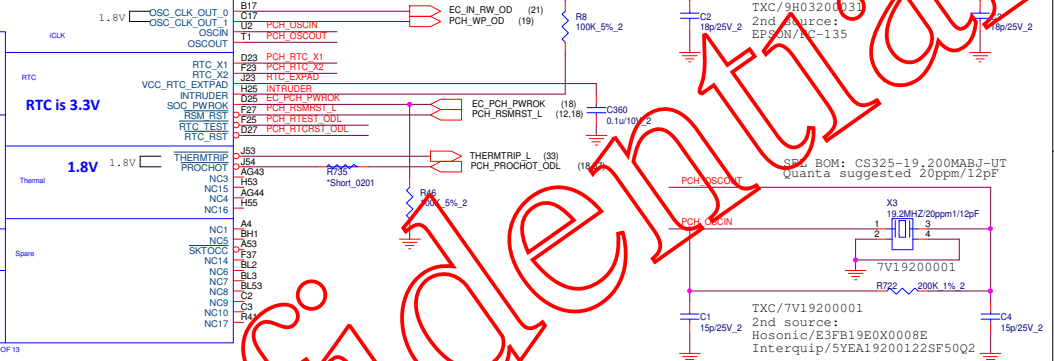
native SD card support dropped

TO-EC

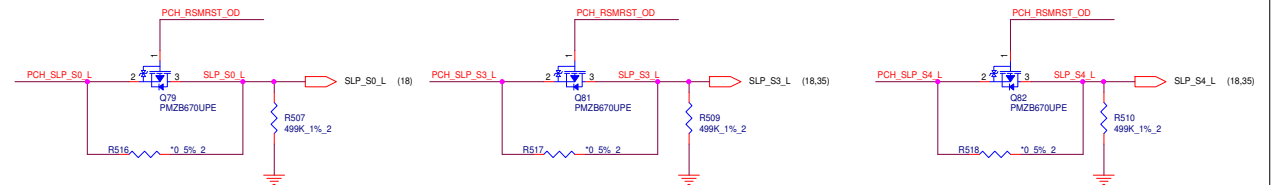
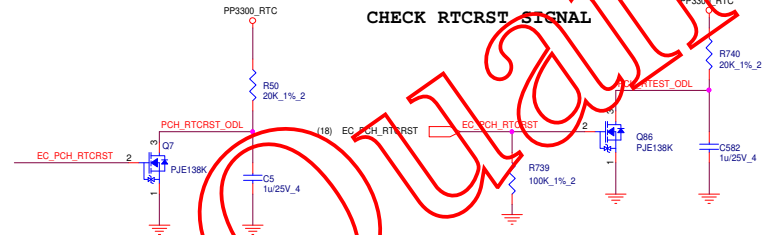
TO-FLASH



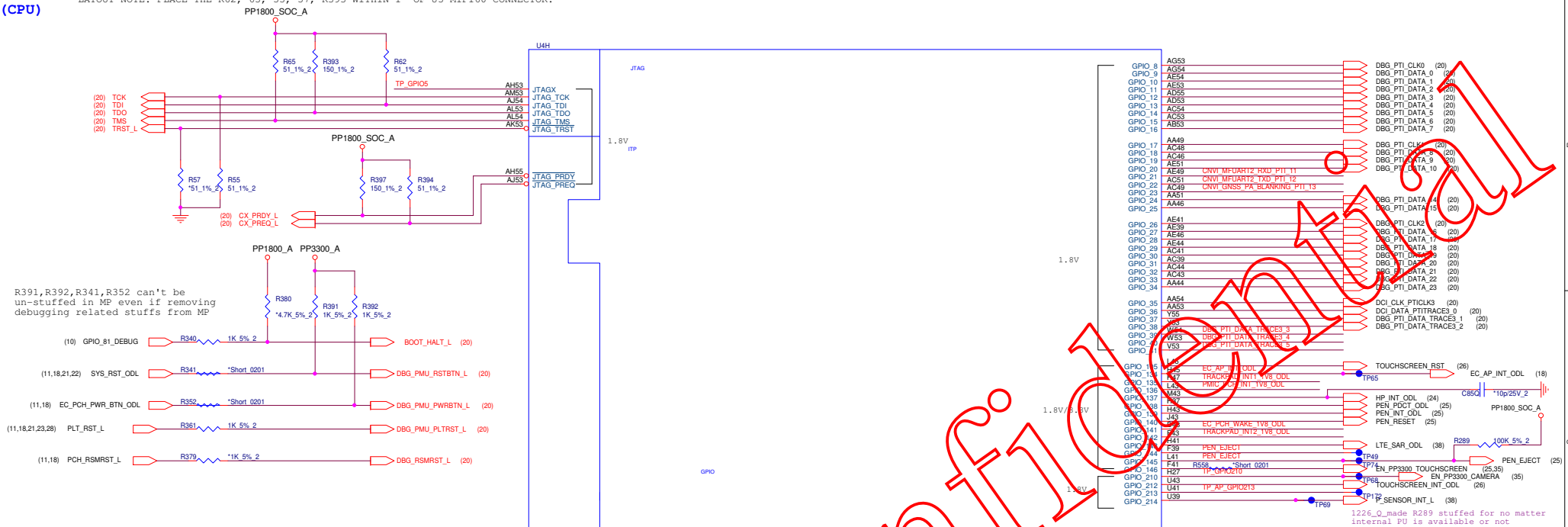




CHECK RTCRST SIGNAL



(CPU)



R391,R392,R341,R352 can't be
un-stuffed in MP even if removing
debugging related stuffs from MP

Timing diagram for the boot sequence. The diagram shows the relationship between various signals and internal components (R340, R341, R352, R361, R379) and their timing relative to the boot sequence. The signals are:

- (10) GPIO_81_DEBUG: Connected to R340. Timing: 1K 5% 2.
- (11,18,21,22) SYS_RST_ODL: Connected to R341. Timing: *Short 0201.
- (11,18) EC_PCH_PWR_BTN_ODL: Connected to R352. Timing: *Short 0201.
- (11,18,21,23,28) PLT_RST_L: Connected to R361. Timing: 1K 5% 2.
- (11,18) PCH_RSMRST_L: Connected to R379. Timing: *1K 5% 2.

The diagram also shows the output signals: BOOT_HALT_L (20), DBG_PMU_RSTBTN_L (20), DBG_PMU_PWRBTN_L (20), and DBG_PMU_PLTRST_L (20).

1226_Q_made R289 stuffed for no matter
internal PU is available or not

PEN_EJECT

C86Q

*10p/25V 2

R524 *Short 0201 TRACKPAD_INT1_IV8_ODL
R531 *Short 0201 TRACKPAD_INT2_IV8_ODL
0102_Q Changed R531 to a short pad

R14 *Short 0201 CNVI_GNSS_PA_BLANKING (28)

R16 *0 5% 2 DBG_PTI_DATA_13 (20)

R17 *Short 0201 CNVI_MFUART2_RXD (28)

R24 *0 5% 2 DBG_PTI_DATA_11 (20)

R25 *Short 0201 CNVI_MFUART2_TXD (28)

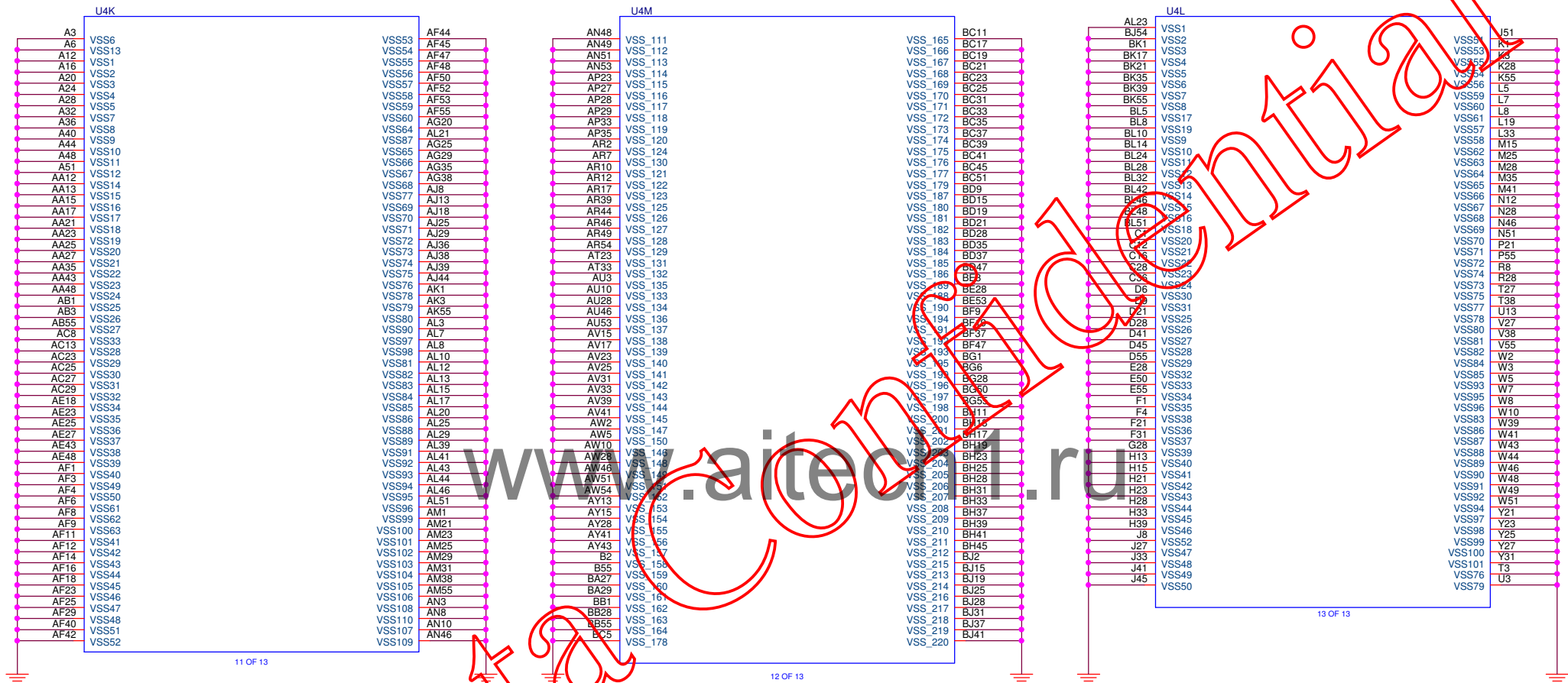
R61 *0 5% 2 DBG_PTI_DATA_12 (20)



```
R380 is reserved for strapping high (GPIO_81)
R877 is for strapping low to not allow eMMC as a boot source (GPIO_27)
No external PU/PD on GPIO_28, using internal PD for allowing SPI as a boot source
```

(CPU)

GLK ULT (GND)



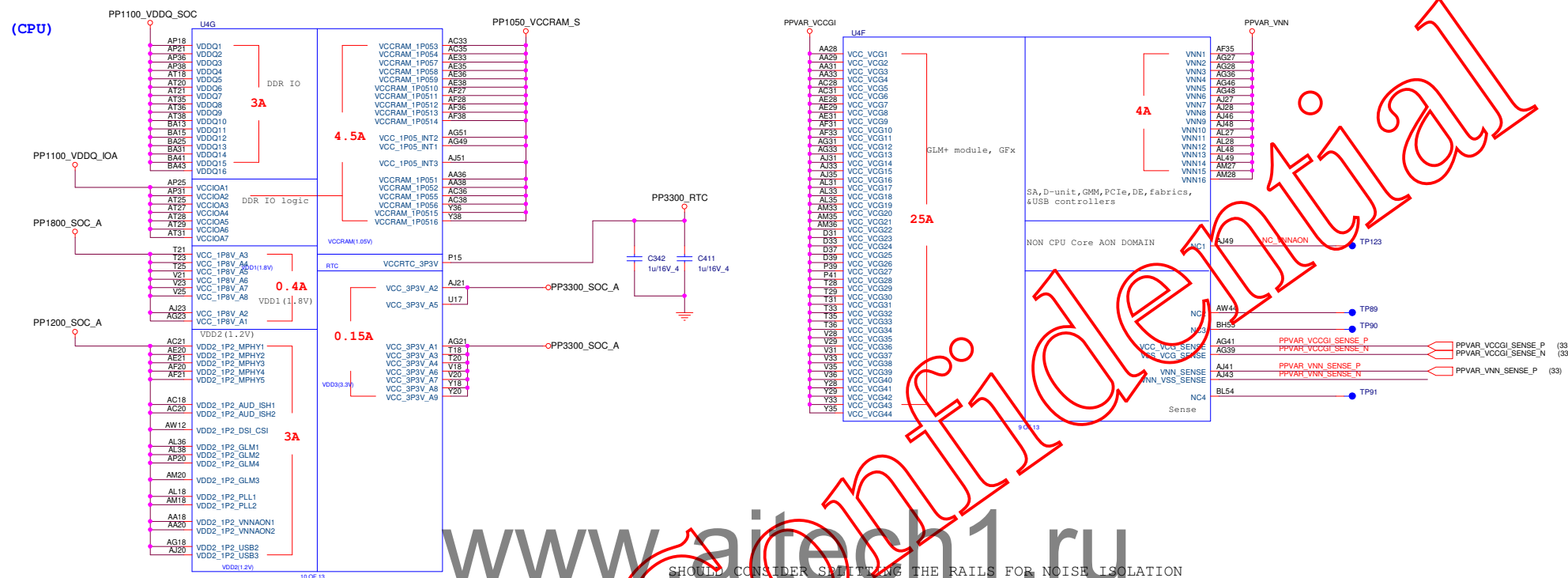
Quanta Computer Inc.

PROJECT : ZAK_ZAN_ZAP_ZAQ

Size	Document Number	Rev
	SOC GROUND	1A
Date:	Wednesday, January 09, 2019	Sheet 13 of 45

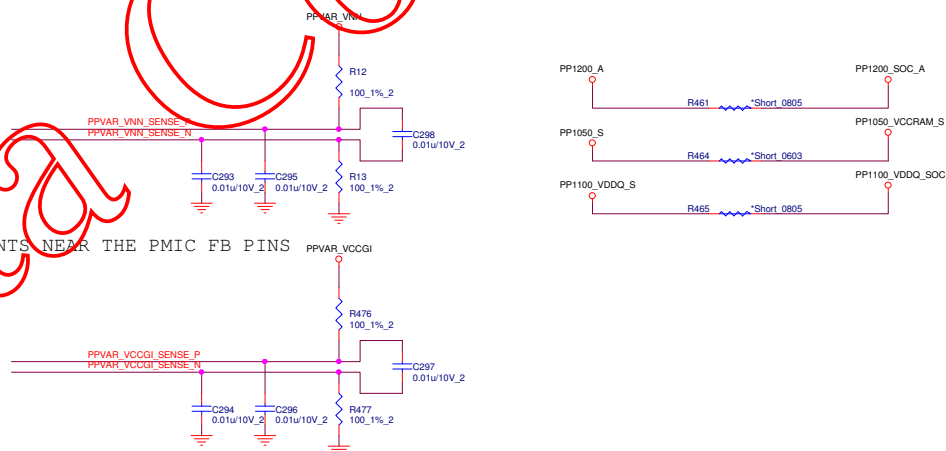
SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION

Gemini (POWER)



SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION

PLEASE THESE COMPONENTS NEAR THE PMIC FB PINS



Quanta Computer Inc.

PROJECT : ZAK_ZAN_ZAP_ZAQ

Size Document Number

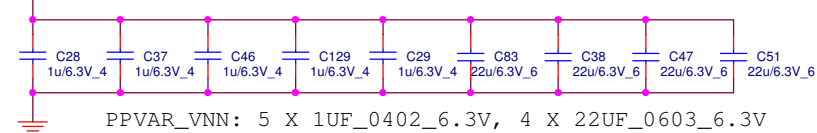
SOC POWER

Date: Wednesday, January 09, 2019 Sheet 14 of 45

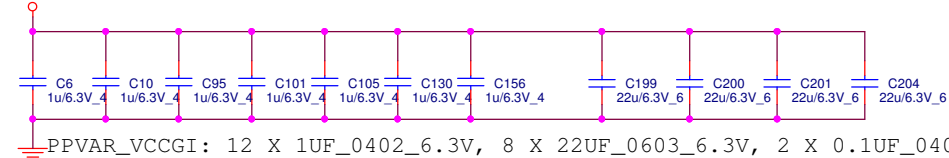
(CPU)

PPVAR_VNN

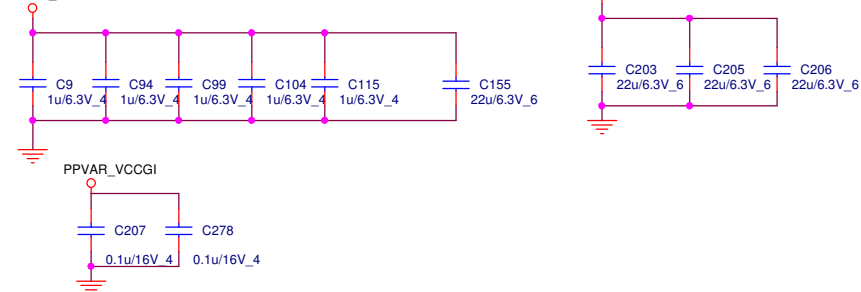
DECOUPLING VALUES AND NUMBER BASED ON THE REFERENCE DOC



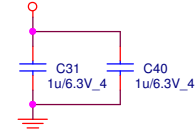
PPVAR_VCCGI



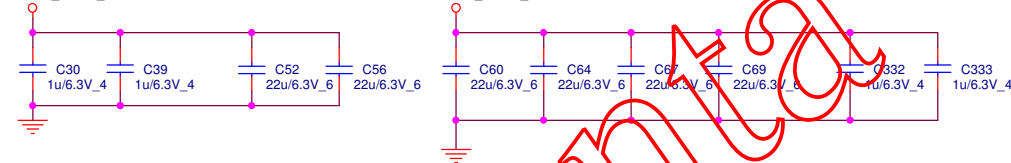
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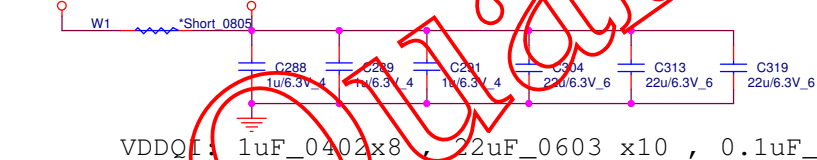
PP1100_VDDQ_SOC



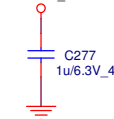
PP1100_VDDQ_SOC



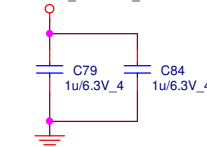
PP1100_VDDQ_S



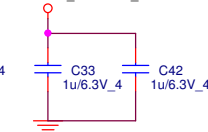
PPVAR_VNN



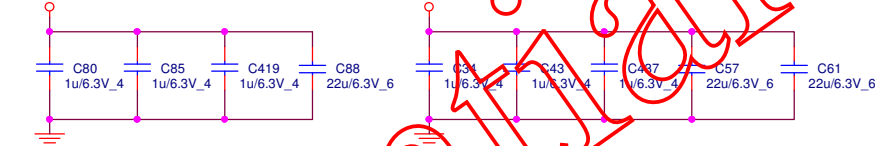
PP1050_VCCRAM_S



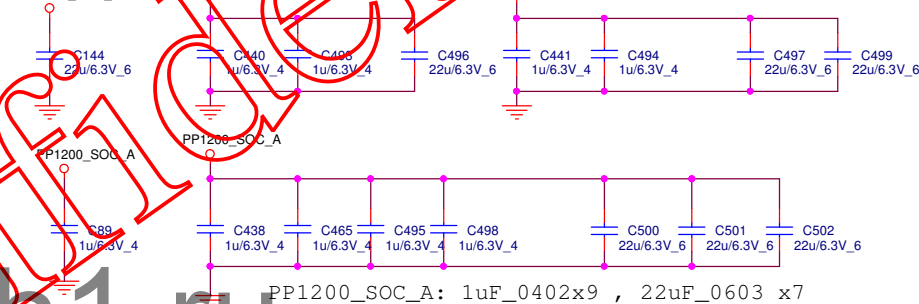
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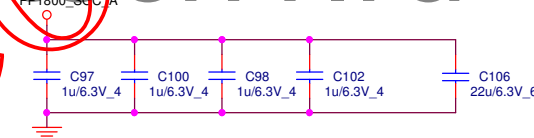
PP1050_VCCRAM_S



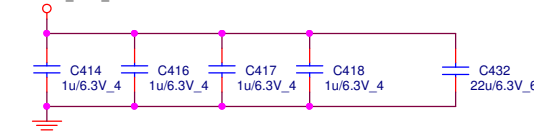
PP1200_SOC_A



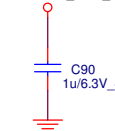
PP1800_SOC_A: 1uF_0402x4, 22uF_0603 x1



PP3300_SOC_A

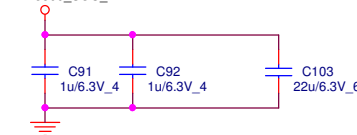


PP3300_SOC_A

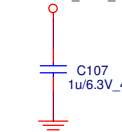


PP3300_SOC_A: 1uF_0402x8, 22uF_0603 x2

PP3300_SOC_A



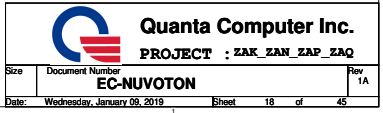
PP3300_SOC_A



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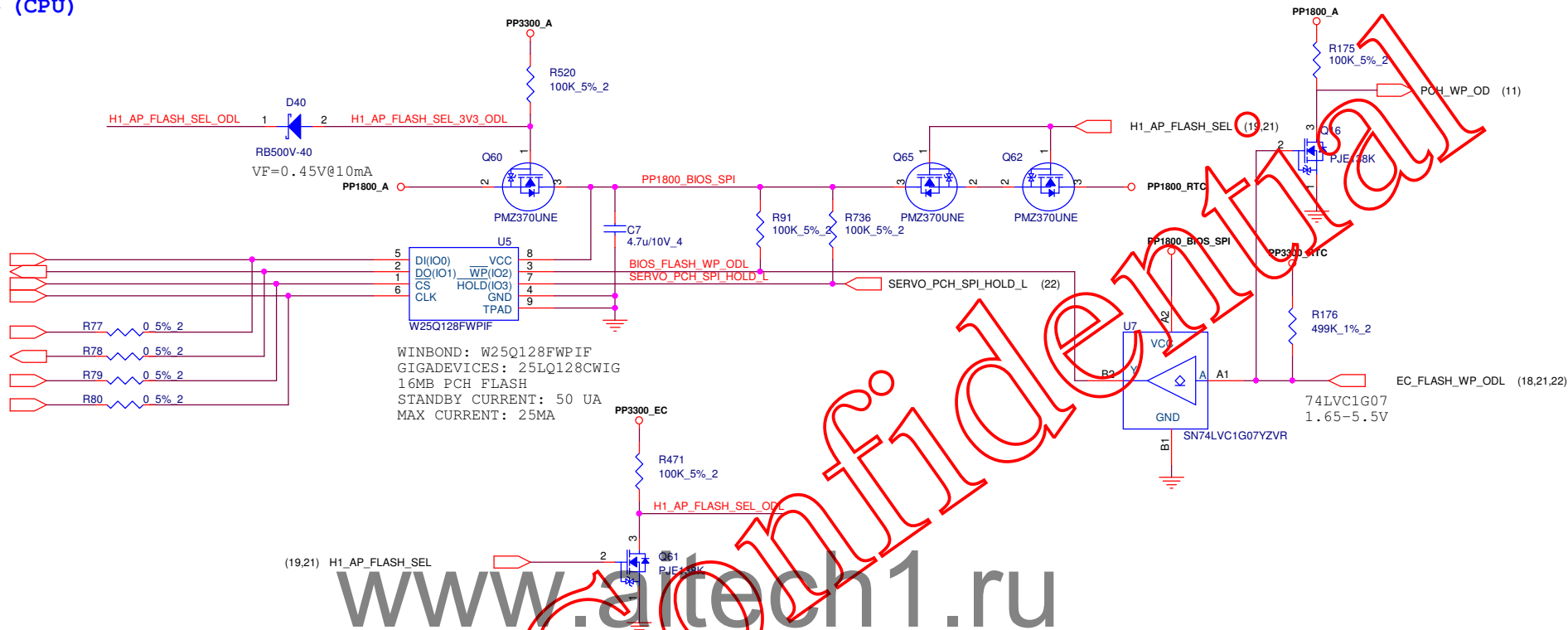
PROJECT : ZAK_ZAN_ZAP_ZAQ

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	SOC DECOUPLING	1A
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PCH SPI FLASH (CPU)

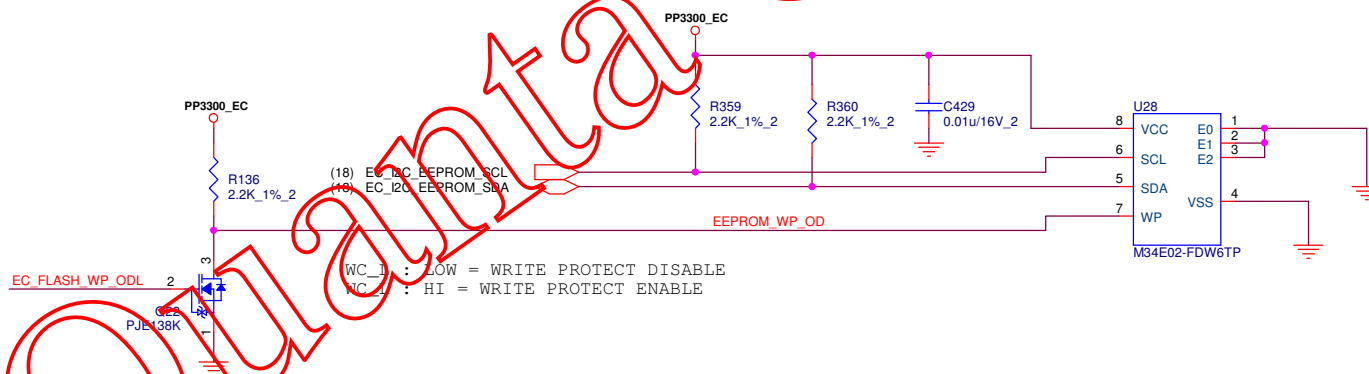
- (9) PCH_SPI_MOSI
- (9) PCH_SPI_MISO_R
- (9) PCH_SPI_CS0_L
- (9) PCH_SPI_CLK
- (21,22) SERVO_PCH_SPI_MOSI
- (21,22) SERVO_PCH_SPI_MISO
- (21,22) SERVO_PCH_SPI_CS_L
- (21,22) SERVO_PCH_SPI_CLK



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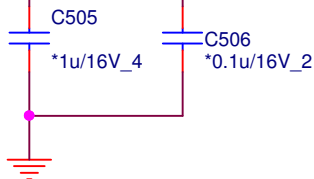
(KBC)

SKU EEPROM



(INT)

PP1800_A

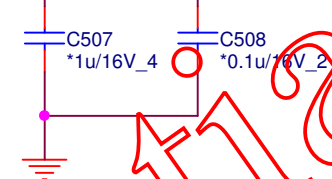


LAYOUT NOTE: PLACING THE SERIAL R'S WITHIN 1 " OF THE DEBUG CONNECTOR

PP1800_A

PP1800_A

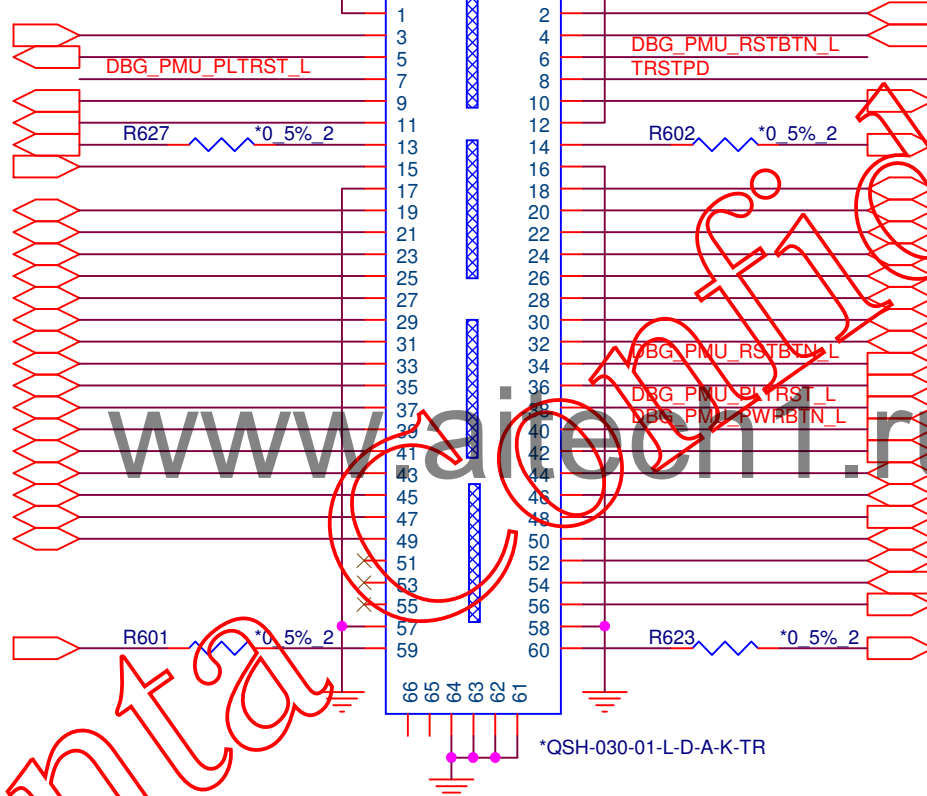
PP1800_A



- (12) TCK
- (12) TDI
- (12) TRST_L
- (12) CX_PRDY_L
- (12) DBG_PTI_CLK0
- (7) GP_INTD_DSI_TE2

- (12) DBG_PTI_DATA_0
- (12) DBG_PTI_DATA_1
- (12) DBG_PTI_DATA_2
- (12) DBG_PTI_DATA_3
- (12) DBG_PTI_DATA_4
- (12) DBG_PTI_DATA_5
- (12) DBG_PTI_DATA_6
- (12) DBG_PTI_DATA_7
- (12) DBG_PTI_DATA_8
- (12) DBG_PTI_DATA_9
- (12) DBG_PTI_DATA_10
- (12) DBG_PTI_DATA_11
- (12) DBG_PTI_DATA_12
- (12) DBG_PTI_DATA_13
- (12) DBG_PTI_DATA_14
- (12) DBG_PTI_DATA_15

(12) DBG_PTI_CLK1



TMS (12)
TDO (12)

DBG_PMU_RSTBTN_L
TRSTPD

CX_PREQ_L (12)
DBG_PTI_CLK2 (12)

R199
*10K_1%_2

DBG_PTI_DATA_16 (12)
DBG_PTI_DATA_17 (12)
DBG_PTI_DATA_18 (12)
DBG_PTI_DATA_19 (12)
DBG_PTI_DATA_20 (12)
DBG_PTI_DATA_21 (12)
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DBG_PTI_DATA_23 (12)
DBG_PTI_DATA_24 (12)
DBG_PTI_DATA_25 (12)
DBG_PTI_DATA_26 (12)
DBG_PTI_DATA_27 (12)
DBG_PTI_DATA_28 (12)
DBG_PTI_DATA_29 (12)
DBG_PTI_DATA_30 (12)
DBG_PTI_DATA_31 (12)
DBG_PTI_DATA_32 (12)
DBG_PTI_DATA_33 (12)
DBG_PTI_DATA_34 (12)
DBG_PTI_DATA_35 (12)
DBG_PTI_DATA_36 (12)
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DBG_PTI_DATA_39 (12)
DBG_PTI_DATA_40 (12)
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DBG_PTI_DATA_47 (12)
DBG_PTI_DATA_48 (12)
DBG_PTI_DATA_49 (12)
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DBG_PTI_DATA_51 (12)
DBG_PTI_DATA_52 (12)
DBG_PTI_DATA_53 (12)
DBG_PTI_DATA_54 (12)
DBG_PTI_DATA_55 (12)
DBG_PTI_DATA_56 (12)
DBG_PTI_DATA_57 (12)
DBG_PTI_DATA_58 (12)
DBG_PTI_DATA_59 (12)
DBG_PTI_DATA_60 (12)

DBG_PMU_RSTBTN_L

C93
*0.01u/16V_2

DBG_PMU_PWRBTN_L

C78
*0.01u/16V_2

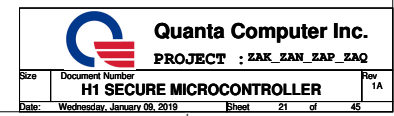
DCI_CLK_PTI_CLK3 (12)



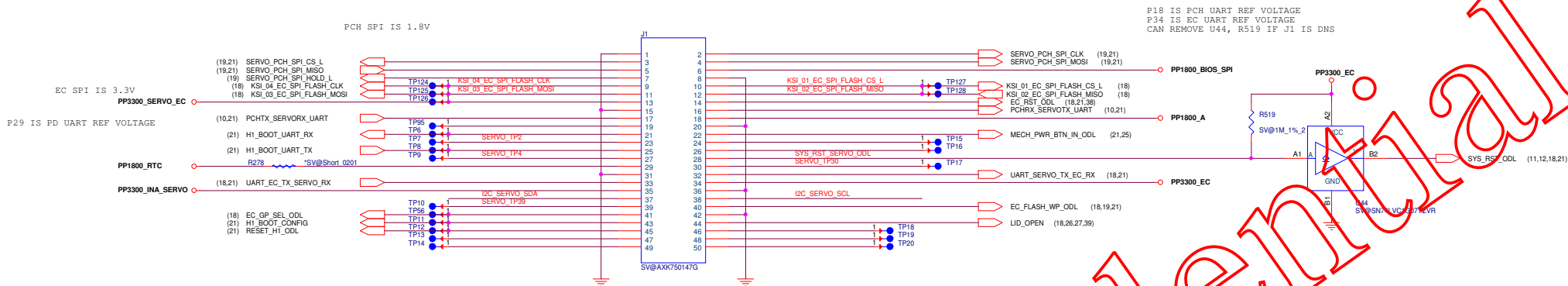
Quanta Computer Inc.

PROJECT : ZAK_ZAN_ZAP_ZAQ

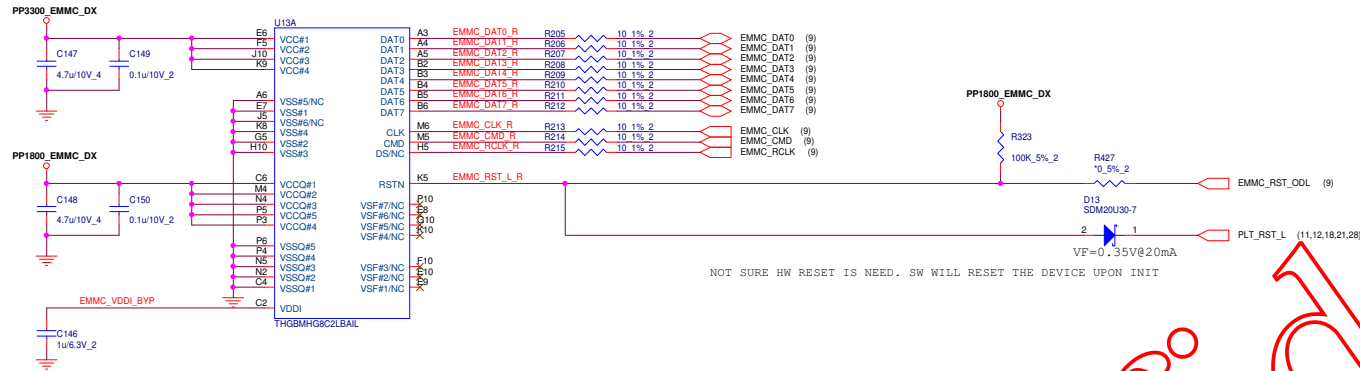
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(GOG)

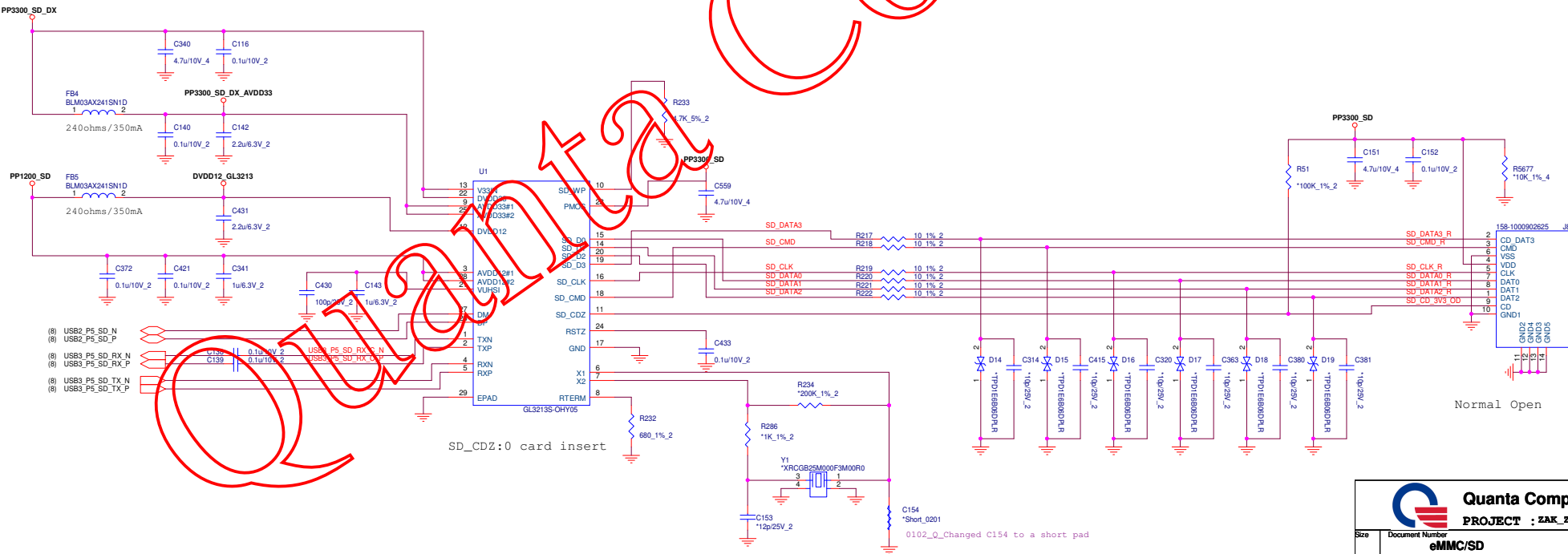


(MMC) 32 GB EMMC STORAGE
150 uA SLEEP CURRENT

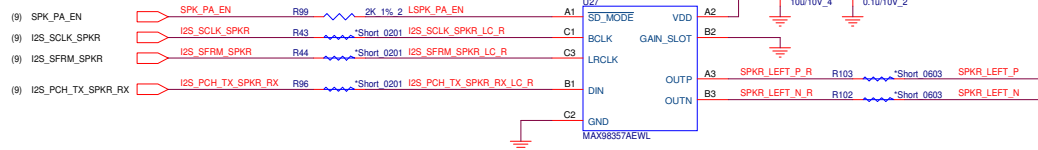


U13B			
A1	NC#A1	NC#H2	H2
A2	NC#A2	NC#H3	H3
A7	RFU#A7/NC	NC#H12	H12
A8	NC#A8	NC#H13	H13
A9	NC#A9	NC#H14	H14
A10	NC#A10	NC#H1	H1
A11	NC#A11	NC#H2	H2
A12	NC#A12	NC#H3	H3
A13	NC#A13	NC#H12	H12
A14	NC#A14	NC#H13	H13
B1	NC#B1	NC#H14	H14
B7	NC#B7	NC#H1	H1
B8	NC#B8	NC#H2	H2
B9	NC#B9	NC#H3	H3
B10	NC#B10	NC#H12	H12
B11	NC#B11	NC#H13	H13
B12	NC#B12	NC#H14	H14
B13	NC#B13	NC#H1	H1
B14	NC#B14	NC#H2	H2
C1	NC#C1	NC#H3	H3
C7	NC#C7	NC#H12	H12
C8	NC#C8	NC#H13	H13
C9	NC#C9	NC#H14	H14
C10	NC#C10	NC#H1	H1
C11	NC#C11	NC#H2	H2
C12	NC#C12	NC#H3	H3
C13	NC#C13	NC#H12	H12
C14	NC#C14	NC#H13	H13
D1	NC#D1	NC#H14	H14
D2	NC#D2	NC#H1	H1
D3	NC#D3	NC#H2	H2
D4	NC#D4	NC#H3	H3
D5	NC#D5	NC#H12	H12
D6	NC#D6	NC#H13	H13
D7	NC#D7	NC#H14	H14
D8	NC#D8	NC#H1	H1
D9	NC#D9	NC#H2	H2
D10	NC#D10	NC#H3	H3
D11	NC#D11	NC#H12	H12
D12	NC#D12	NC#H13	H13
D13	NC#D13	NC#H14	H14
D14	NC#D14	NC#H1	H1
E1	NC#E1	NC#H2	H2
E2	NC#E2	NC#H3	H3
E3	NC#E3	NC#H12	H12
E4	NC#E4	NC#H13	H13
E5	NC#E5	NC#H14	H14
E6	NC#E6	NC#H1	H1
E7	NC#E7	NC#H2	H2
E8	NC#E8	NC#H3	H3
E9	NC#E9	NC#H12	H12
E10	NC#E10	NC#H13	H13
E11	NC#E11	NC#H14	H14
E12	NC#E12	NC#H1	H1
E13	NC#E13	NC#H2	H2
E14	NC#E14	NC#H3	H3
F1	NC#F1	NC#H12	H12
F2	NC#F2	NC#H13	H13
F3	NC#F3	NC#H14	H14
F4	NC#F4	NC#H1	H1
F5	NC#F5	NC#H2	H2
F6	NC#F6	NC#H3	H3
F7	NC#F7	NC#H12	H12
F8	NC#F8	NC#H13	H13
F9	NC#F9	NC#H14	H14
F10	NC#F10	NC#H1	H1
F11	NC#F11	NC#H2	H2
F12	NC#F12	NC#H3	H3
F13	NC#F13	NC#H12	H12
F14	NC#F14	NC#H13	H13
G1	NC#G1	NC#H14	H14
G2	NC#G2	NC#H1	H1
G3	NC#G3	NC#H2	H2
G4	NC#G4	NC#H3	H3
G5	NC#G5	NC#H12	H12
G6	NC#G6	NC#H13	H13
G7	NC#G7	NC#H14	H14
G8	NC#G8	NC#H1	H1
G9	NC#G9	NC#H2	H2
G10	NC#G10	NC#H3	H3
G11	NC#G11	NC#H12	H12
G12	NC#G12	NC#H13	H13
G13	NC#G13	NC#H14	H14
G14	NC#G14	NC#H1	H1
H1	NC#H1		

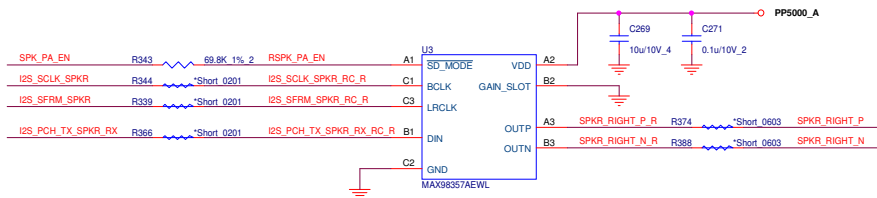
(CRD) MICRO SD CARD



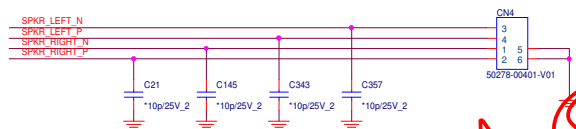
(AMP)



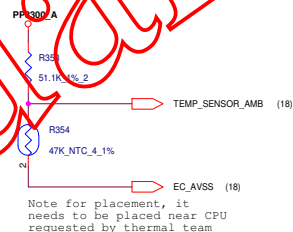
RIGHT CHANNEL



(ADO)

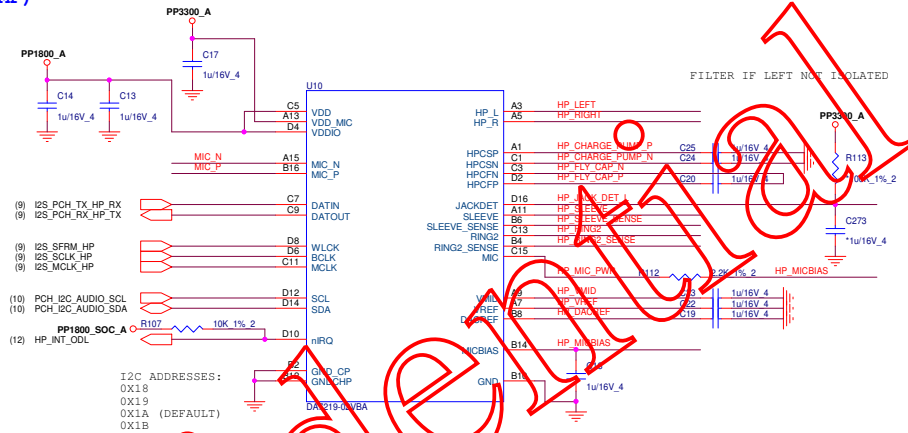


(THM)

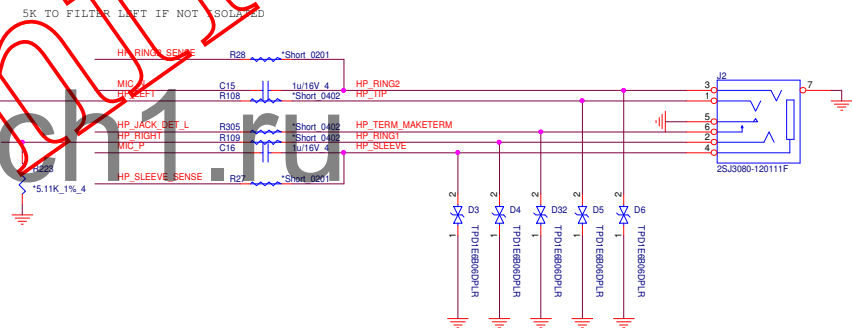


CSP PACKAGE, BUT CAN BE ROUTED ON TYPE-3
<10UA IN DEEP SLEEP

(AMP)



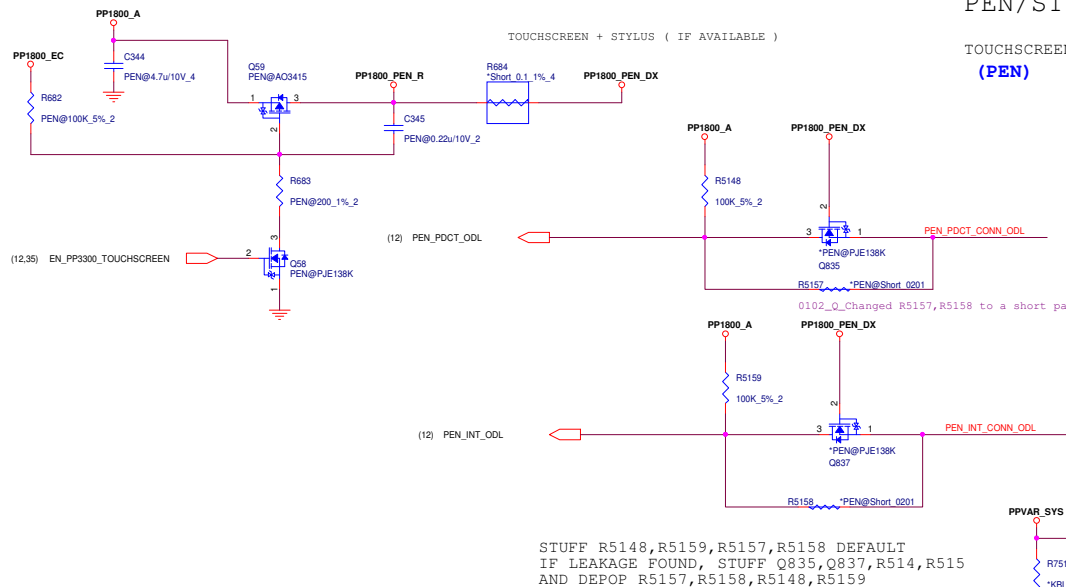
(ADO)



CHANGED MIC SERIES CAPS TO 1UF TO MATCH 10HZ 3DB
FREQUENCY RECOMMENDED IN THE DA7219 DATASHEET

THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL
THE SAME APPLIES TO HP_SLEEVE AND HP_SLEEVE_SENSE SIGNALS
ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

(PEN)

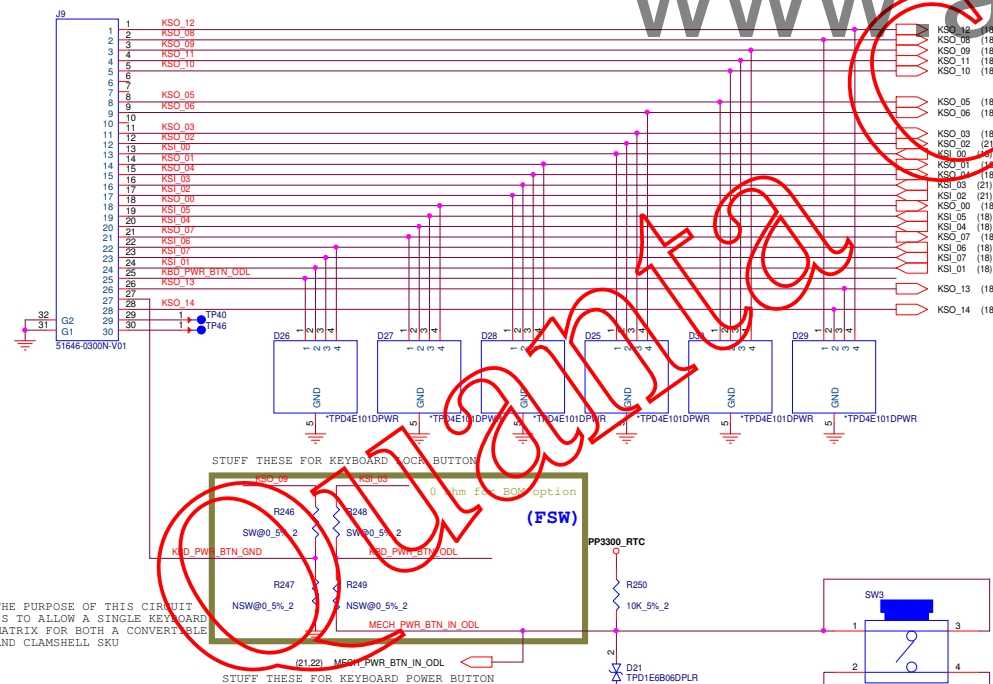


STUFF R5148,R5159,R5157,R5158 DEFAULT
IF LEAKAGE FOUND, STUFF Q835,Q837,R514,R515
AND DEPOP R5157,R5158,R5148,R5159

(KBC)

KEYBOARD

CM TO CHOOSE CONNECTOR- THIS ONE WILL SUPPORT THE KEYPAD SO THE PINOUT MAY NEED TO CHANGE

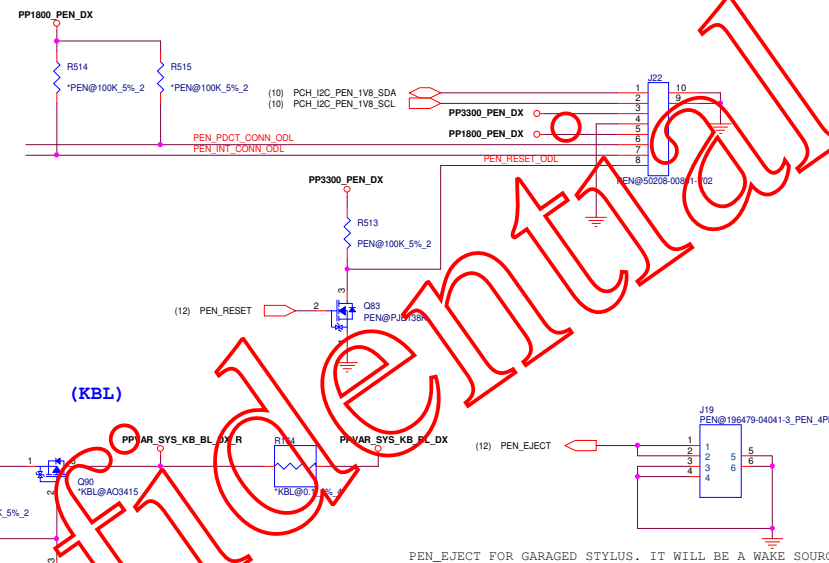


THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHHELL SKU

Convertible	R246,R248,SW3 STUFF ; R247,R249 NC
Clamshell	R247,R249 STUFF ; R246,R248,SW3 NC

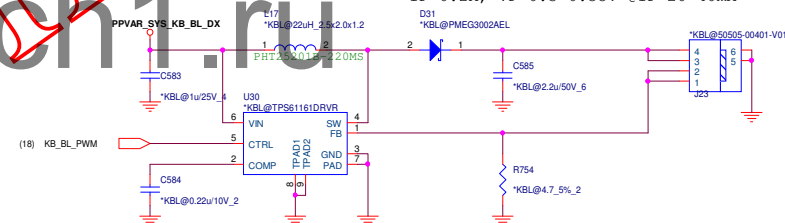
PEN/STYLUS CONNECTOR

PEN 7-BIT I2C ADDRESS = 0X09
~ 100 MA



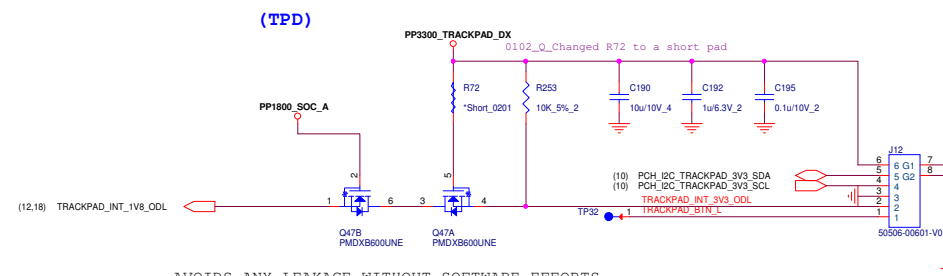
PEN_EJECT FOR GARAGED STYLUS. IT WILL BE A WAKE SOURCE

KEYBOARD BACKLIGHT CONN
IF=0.2A, VF=0.3~0.35V @IF=20~40mA



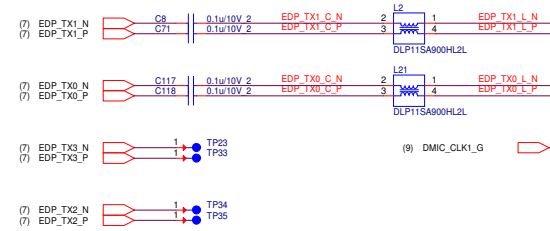
TRACKPAD CONNECTOR

CM TO CHOOSE CONNECTOR



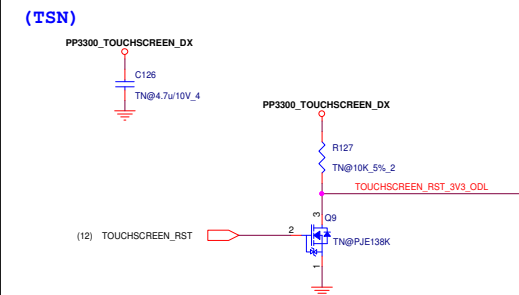
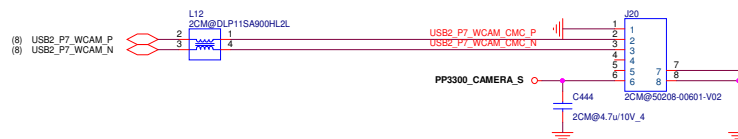
AVIODS ANY LEAKAGE WITHOUT SOFTWARE EFFORTS

EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR

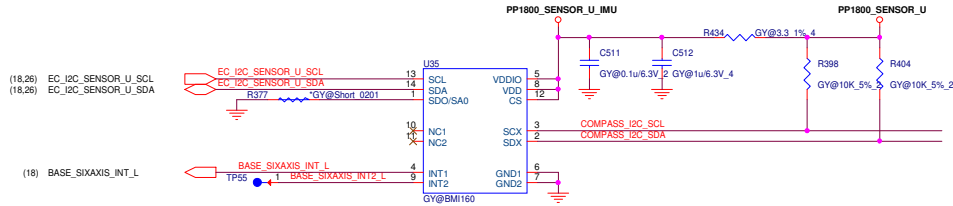


```
I2C MODE: ( SET BY NCS TIE TO VDDIO )
I2C 8bit ADDRESS: 0X3E (SDO_ADDR = VDDIO)
I2C MAX SPEED = 3.4MHZ
```

WFC INTERFACE PINOUT TBD. PENDING CHANGE



(GRS)



IMU

MODE 2 (SLAVE TO EC, MASTER TO MAG)
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 7'0X68 (LSB SET BY SD0/SA0) -->8'0XD0h

(ACM)

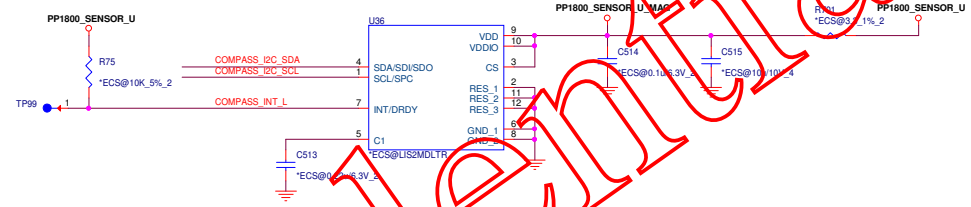
0 ohm for BOM option

R30Q~R32Q place near to IMU U35

EC_I2C_SENSOR_U_SCL R30Q ACM@0.5% 2 EC_I2C_SENSOR_U_SCL_WFC (40)
EC_I2C_SENSOR_U_SDA R31Q ACM@0.5% 2 EC_I2C_SENSOR_U_SDA_WFC (40)
BASE_SIXAXIS_INT_L R32Q ACM@0.5% 2 BASE_SIXAXIS_INT_L_WFC (40)

for AR Camera, IMU can be DNS, but R30Q,R31Q,R32Q need to be stuffed

(ECS)

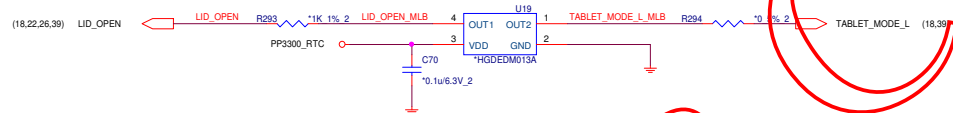


MAGNETOMETER

SLAVE TO IMU SENSOR
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 011B

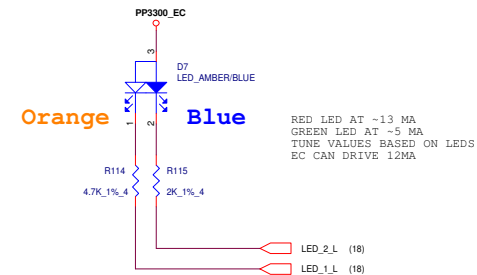
GMR SENSOR (RESERVED FOR ON BOARD SITUATION)

(GMR_MLB) For on board GMR



MAKE SURE TO CHECK THE POLARITY OF MAGNET TO ASSIGN THE PIN LID_OPEN AND TABLET-MODE
IF THE GMR SENSOR IS NOT PLACED ON THE MLB, PLEASE CAREFULLY PLAN THE PINOUT ON THE SUB-BOARD INTERFACE.

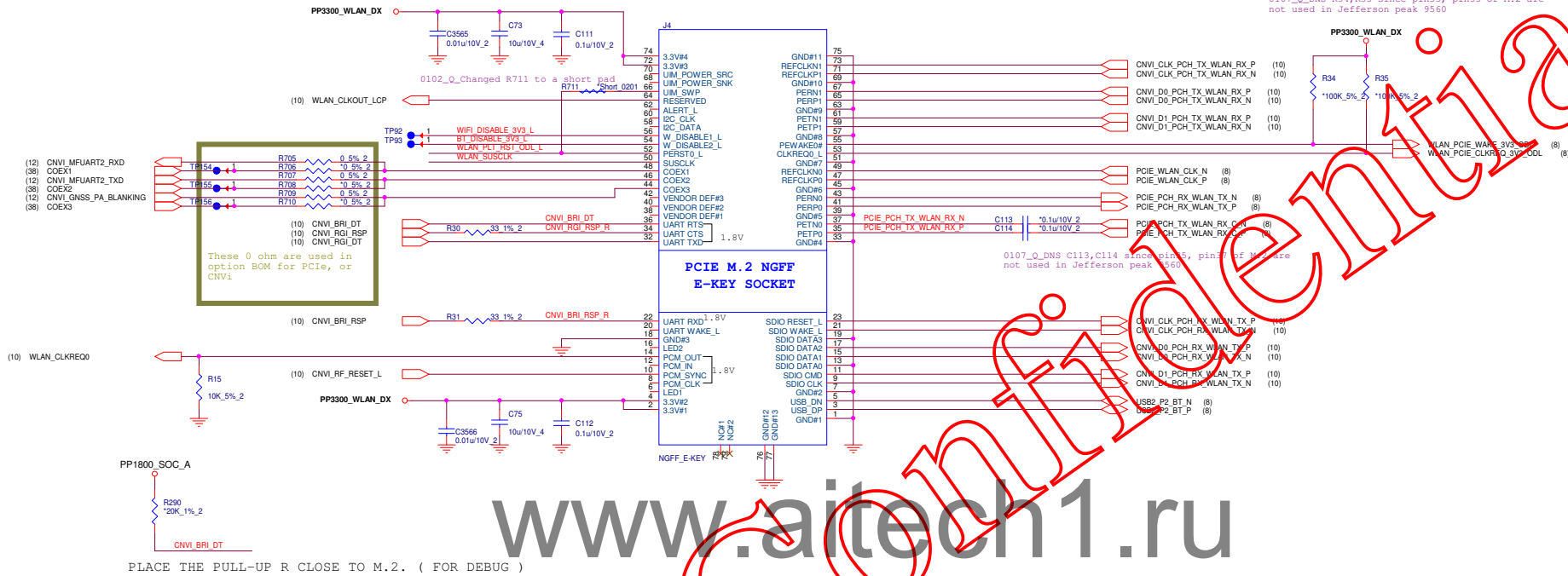
CHARGE/BATTERY LED



WIFI

CM TO CHOOSE CONNECTOR

(NGF)



U46,R38,D9,Q45,C113,C114,R34,R35,Q1,Q2 need to be stuffed for WiFi flexible design

(UTC1)

FOR USB-C PORT 0

TO MIB CONNECTOR

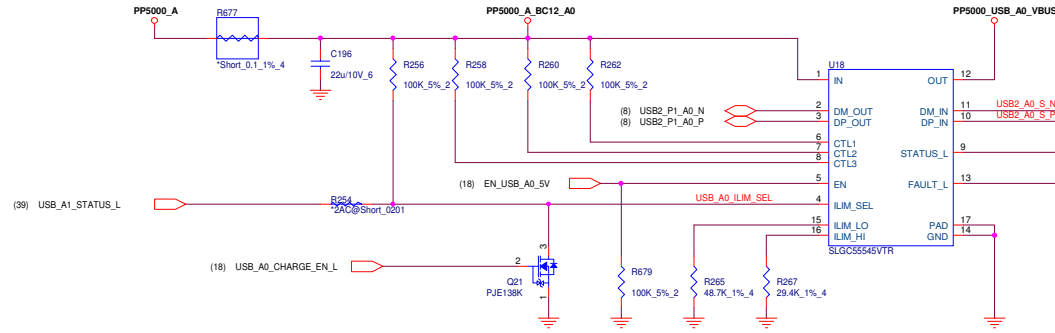
WITH THE NX20P3483, THE VBUS DISCHARGE CAN BE SW CONTROL

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USB_C0_PD_RST IS ACTIVE HIGH WITH 100K INTERNAL PD

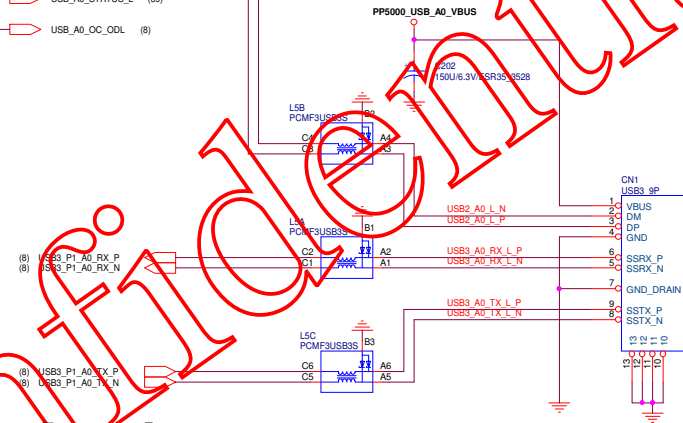
BC 1.2 FOR THE TYPE-A PORT A0

(UBC1)



(UB31)

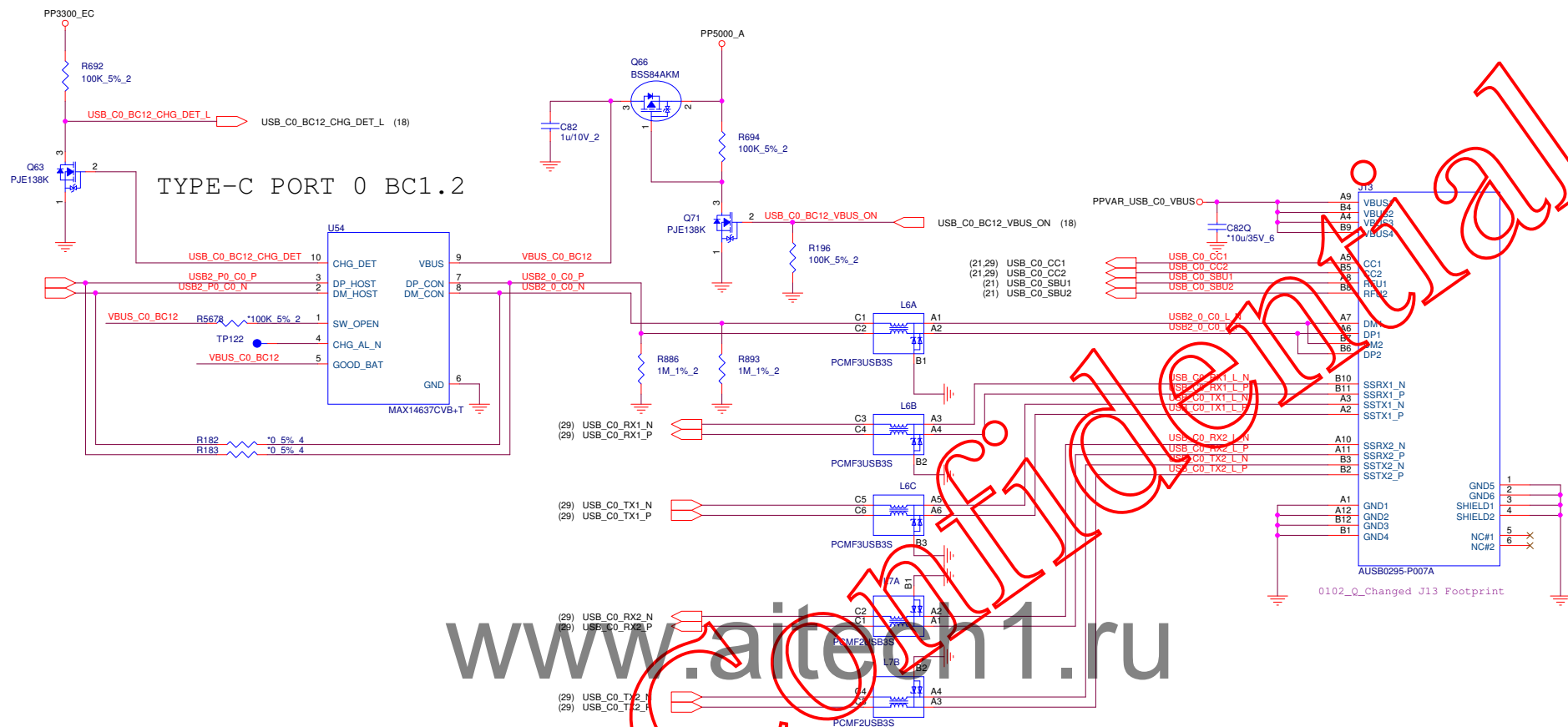
CM TO CHOOSE CONNECTOR



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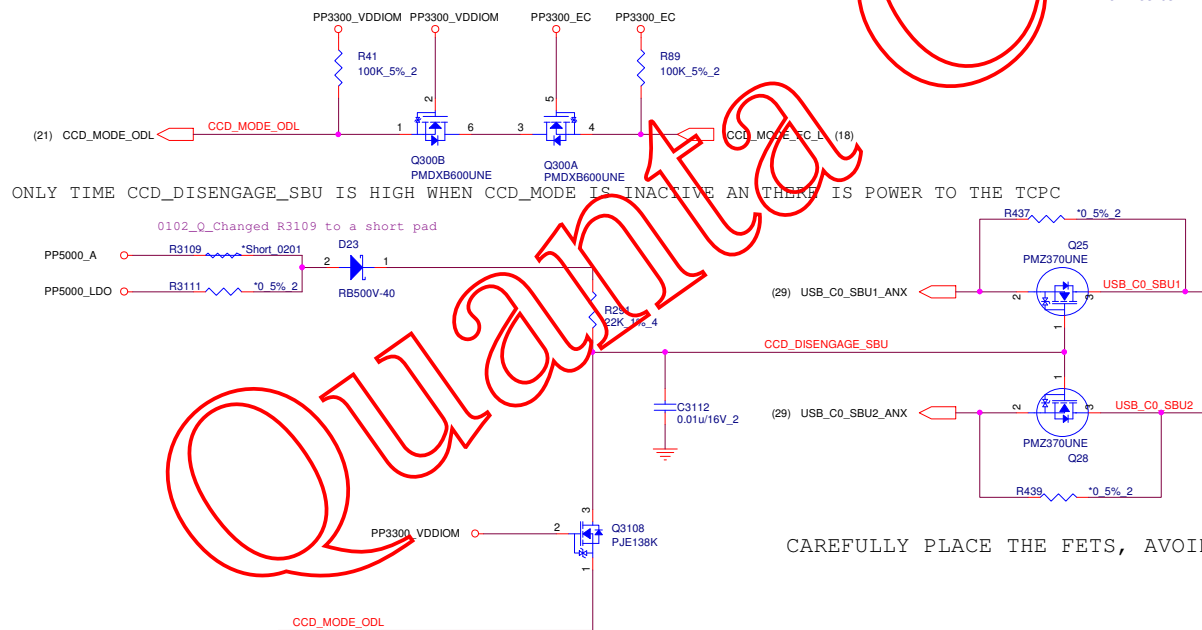
Quanta

(UTC1)

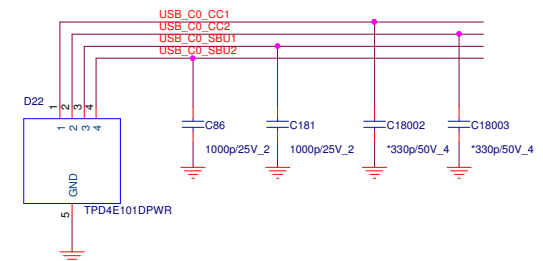


(29) USB_C0_RX2_N
(26) USB_C0_RX2_P

C2
C1
A2
A1
PMP2_SBS
L78
B2

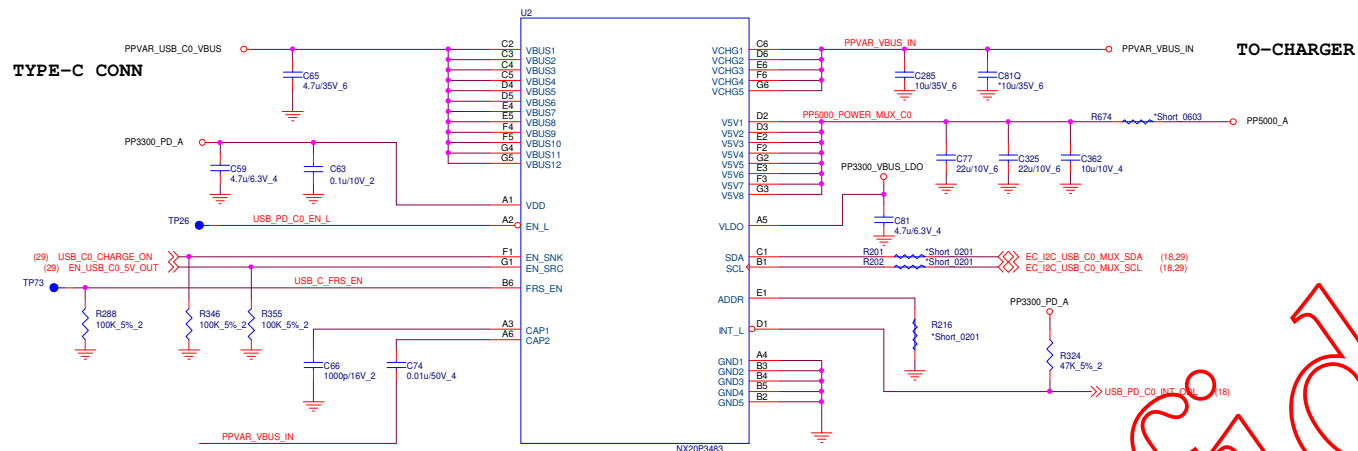


CAREFULLY PLACE THE FETS, AVOID LONG STUB

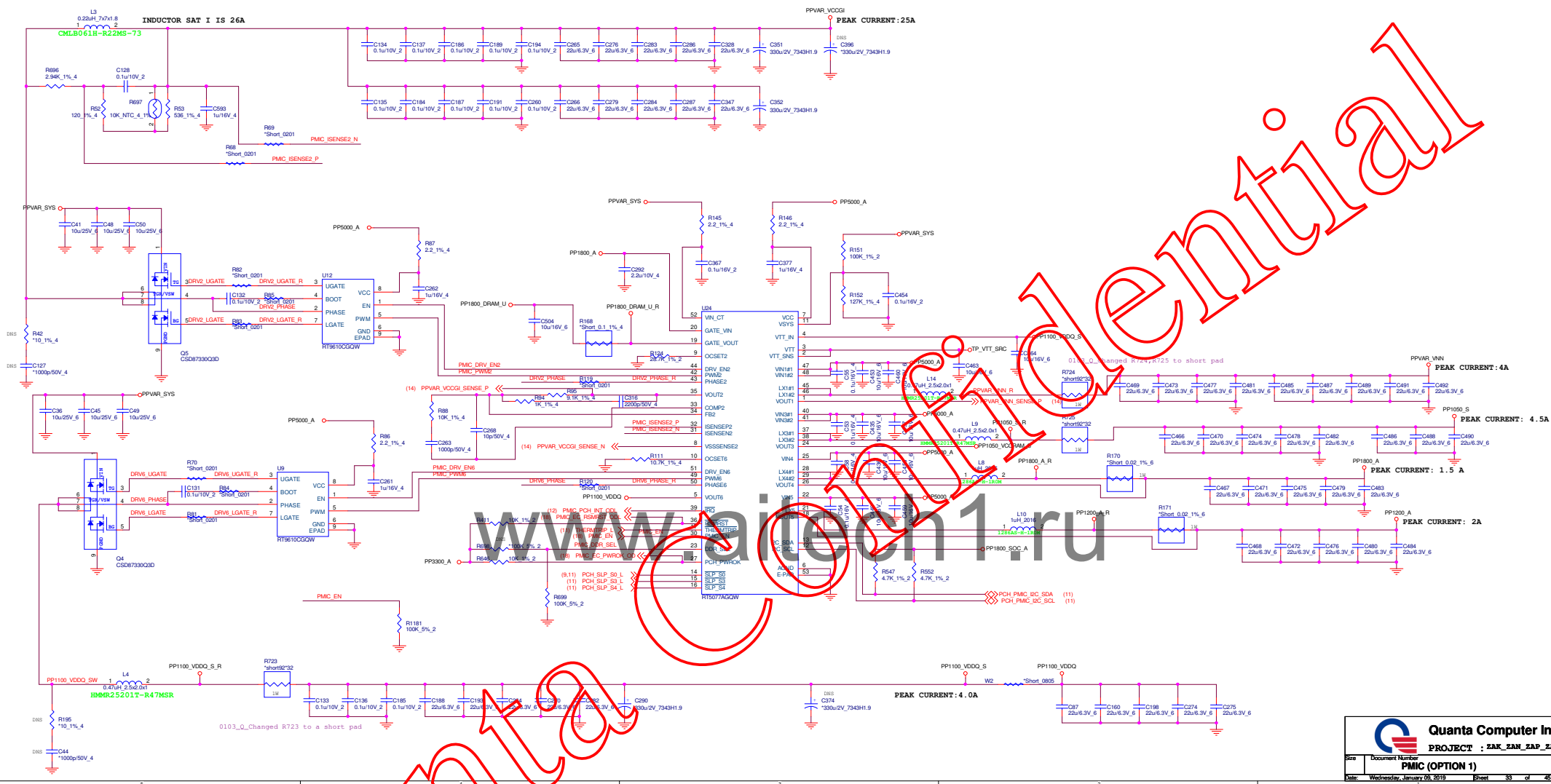


(PUB1)

PORT 0
PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



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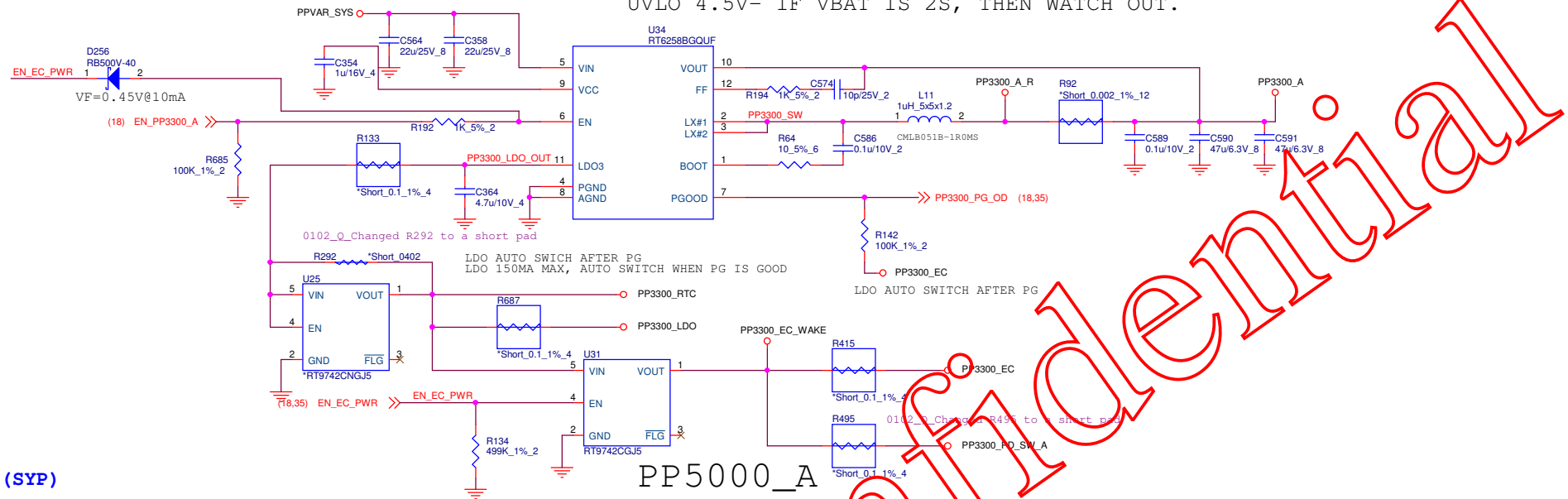


(SYP)

PP3300_A

UVLO 4.5V- IF VBAT IS 2S, THEN WATCH OUT.

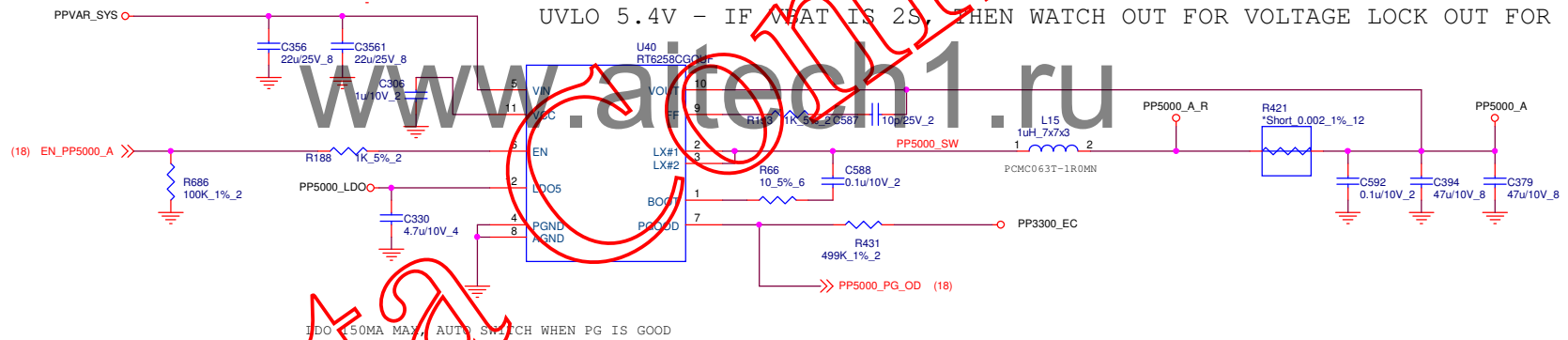
34



(SYP)

PP5000_A

UVLO 5.4V - IF VBAT IS 2S, THEN WATCH OUT FOR VOLTAGE LOCK OUT FOR 1.8V

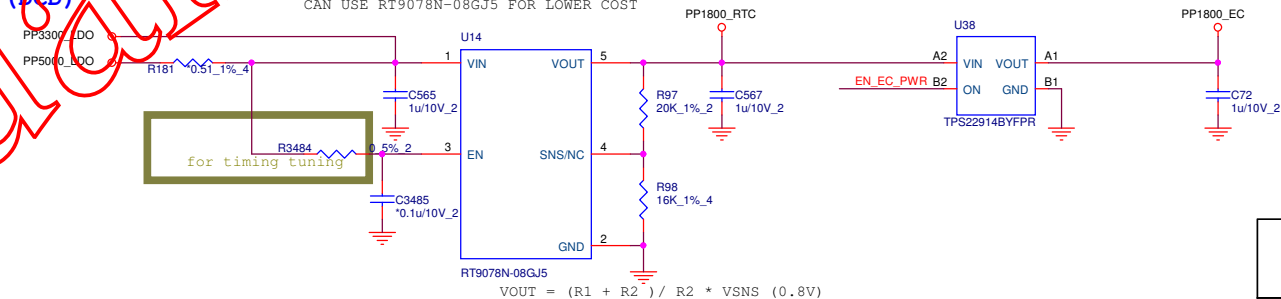


PP1800_RTC, PP1800_EC

PP1800_RTC CAN BE GENERATED BY A SEPARATE DC-DC R
CAN USE RT9078N-08GJ5 FOR LOWER COST

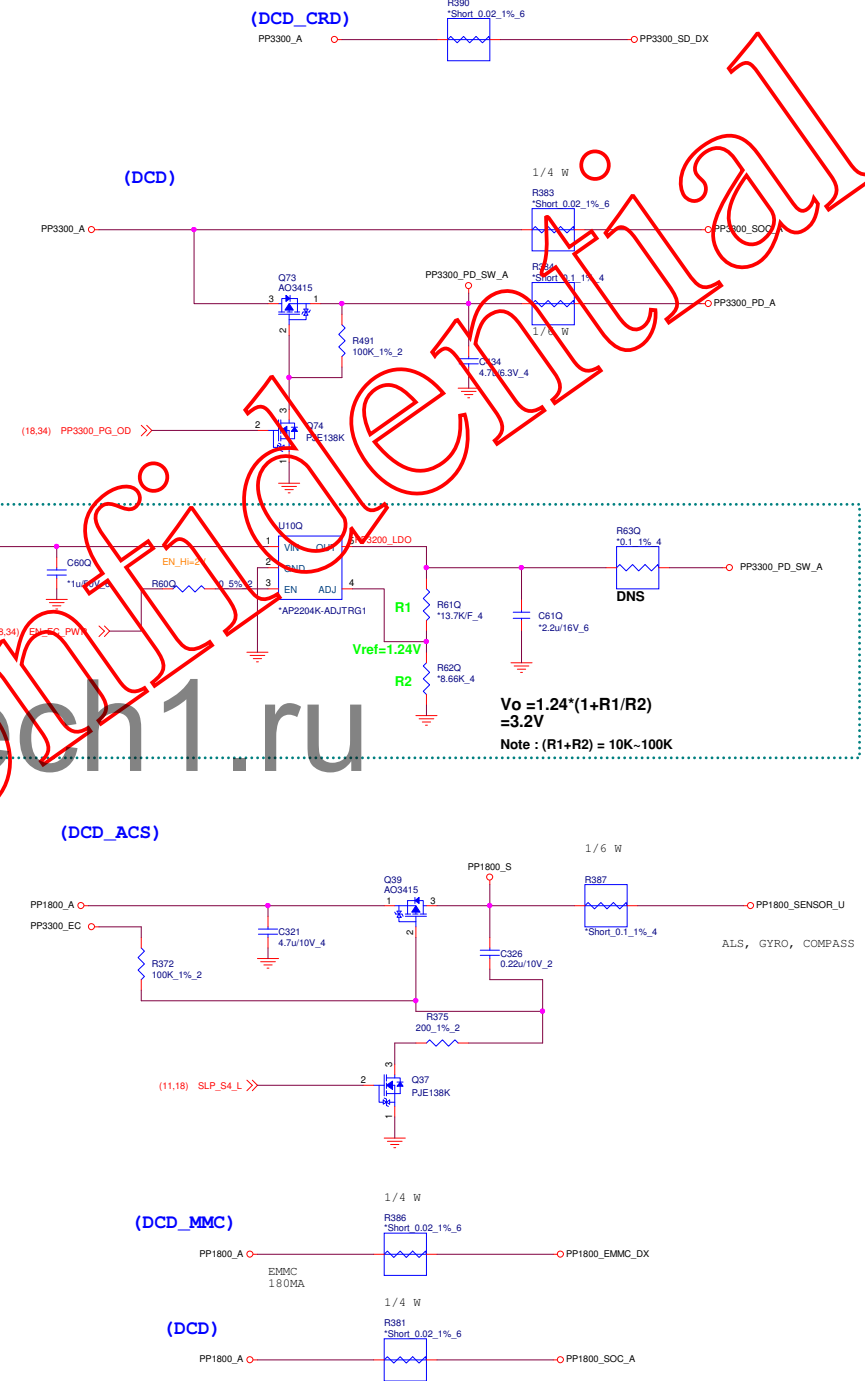
PP1800_EC CAN BE GENERATED BY A SEPARATE REGULATOR

(DCD)

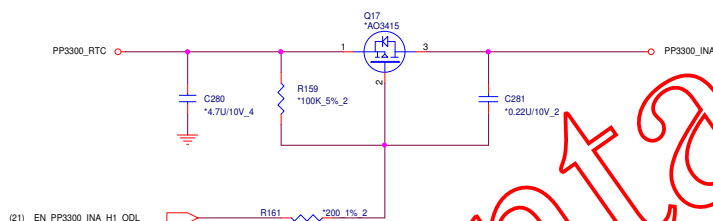
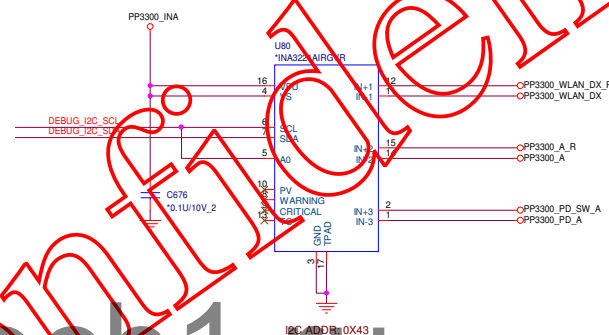
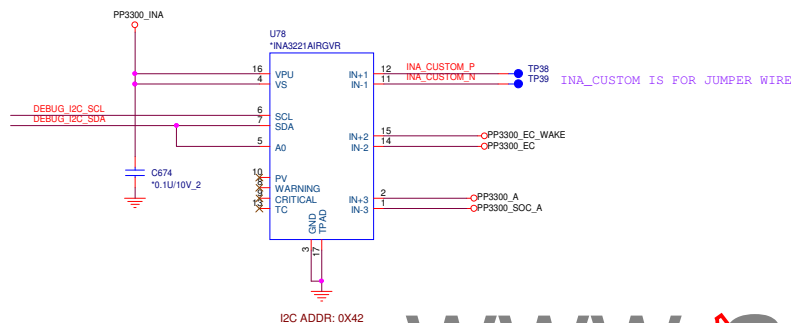
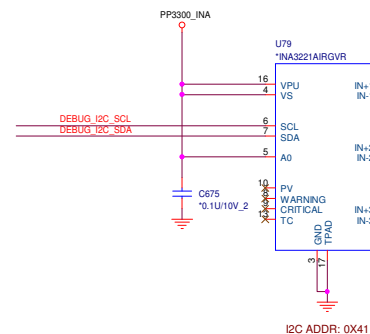
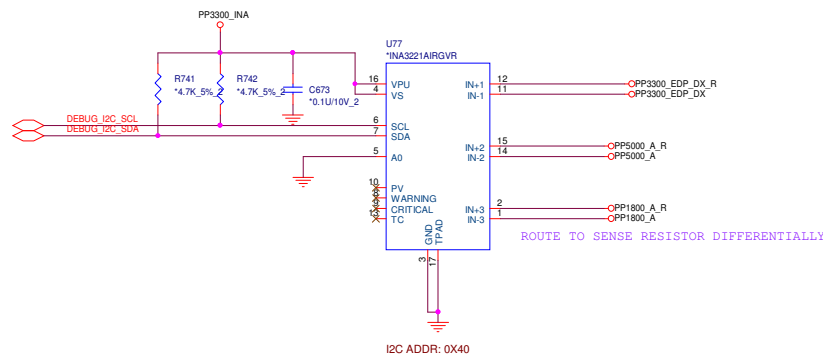


$$VOUT = (R1 + R2) / R2 * VSNS (0.8V)$$

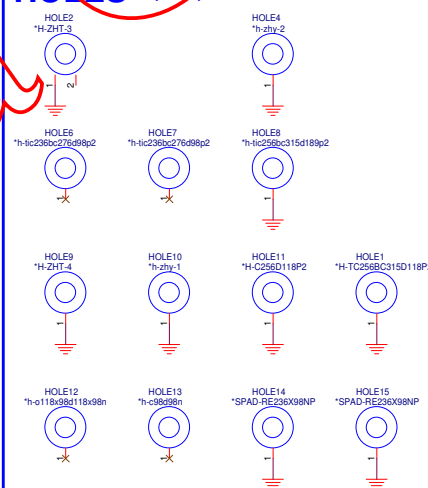
CHOICES FOR THE REGULATORS CAN BE SUBSTITUE AFTER CONFIRM THE FUNCTIONALITY.



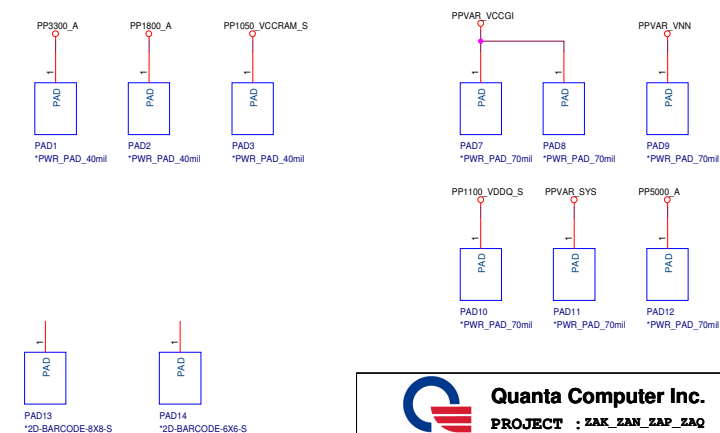
(INA)



HOLES (OTH)



POWER TEST PAD (OTH)



INTERSIL BUCK - BOOST CHARGER

INCREASE OR ADD POSCAPS IF AUDIBLE NOISE IS HEARD

RECOMMENDED VALUE
FROM DATASHEET

RECOMMENDED VALUE
FROM DATASHEET

REQUIRE HIGHER
OUTPUT CAPACITANCE

RATING
HIGH ENOUGH?

I2C ADDR : 0X12

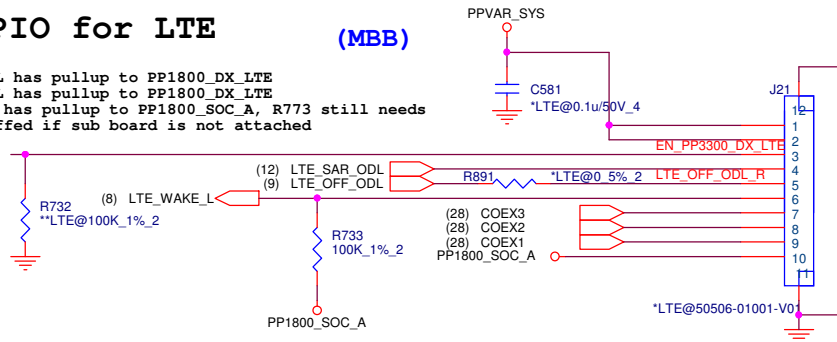
CV: 12.6V
3S1P Battery

GPIO for LTE

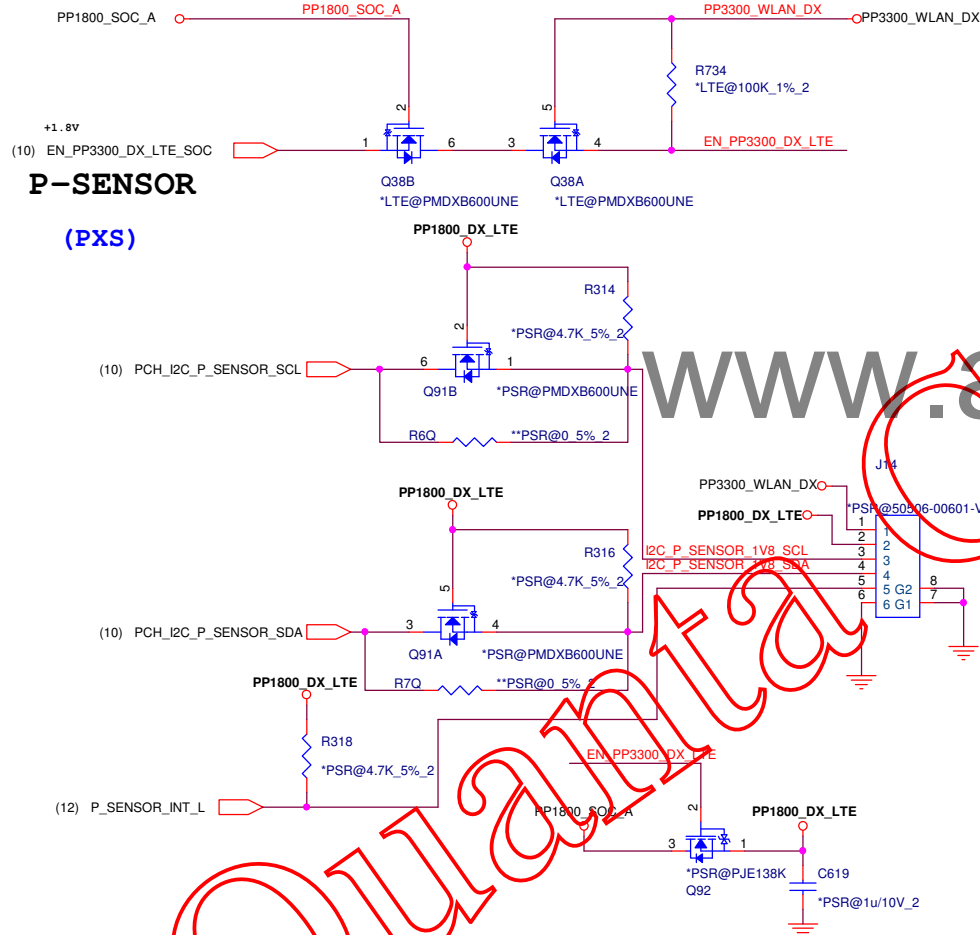
(MBB)

Coral sub board

- LTE_SAR_ODL has pullup to PP1800_DX_LTE
- LTE_OFF_ODL has pullup to PP1800_DX_LTE
- LTE_WAKE_L has pullup to PP1800_SOC_A, R773 still needs to be stuffed if sub board is not attached



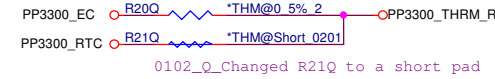
LEVERAGING CORAL BOARD!



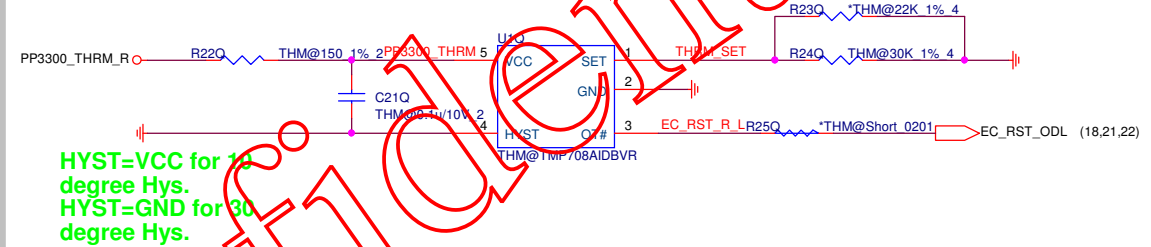
(SYS_THM)

Thermal Protector

Need fine tune
for thermal protect point
Note placement position
TEMP=76.3C



$$R_{set}(Kohm) = 0.0012T^2 - 0.9308T + 96.147$$



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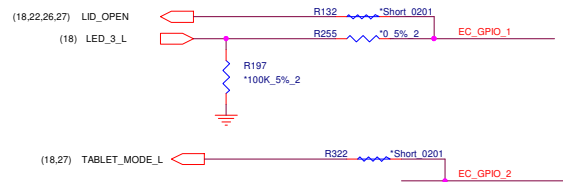
Quanta Computer Inc.

PROJECT : ZAK_ZAN_ZAP_ZAQ

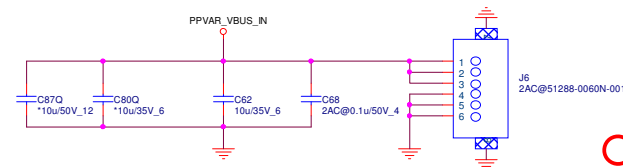
Size	Document Number	Rev
	LTE\$TEST	1A

Date: Wednesday, January 09, 2019 Sheet 38 of 45

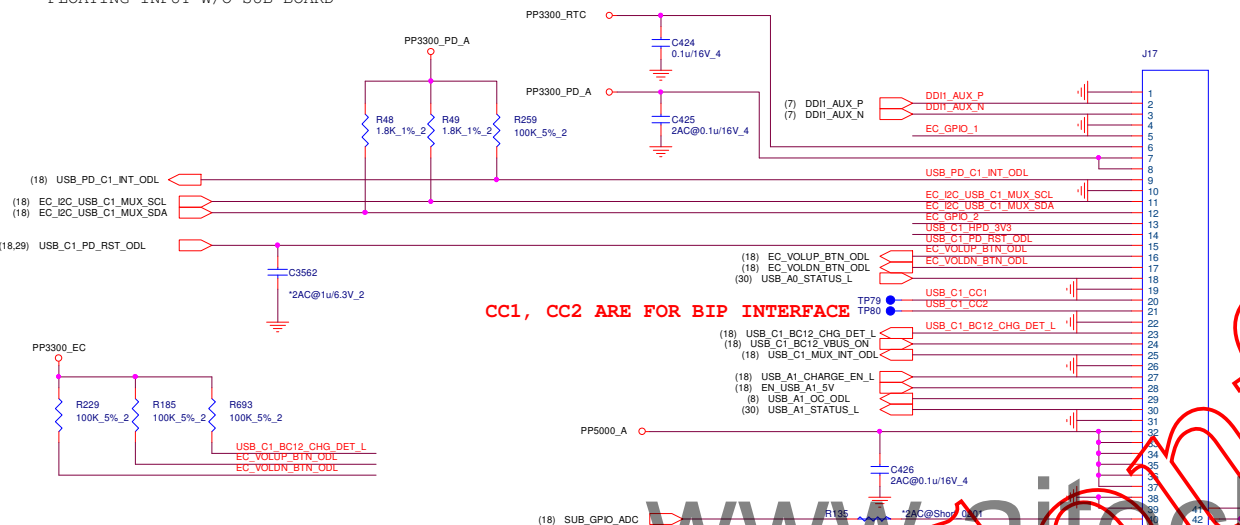
(UTC2)



EC_GPIO1,2 CAN BE USED FOR CONNECTING THE GMR SENSOR ON THE SUB-BOARD
OR IT CAN BE USED TO CONNECT AN SPARE EC GPIO PINS FOR ADDITIONAL CONTROL FROM EC



PULL-DOWN RESISTORS TO AVOID
FLOATING INPUT W/O SUB-BOARD



CC1, CC2 ARE FOR BIP INTERFACE

SUB_GPIO_ADC GOES TO AN ADC PIN OF EC WITH STUFFING OPTIONS
THE PIN CAN BE USED FOR VBUS DETECT OR FOR BOARD ID DETECT, OR USE AS A GENERAL GPIO FROM EC

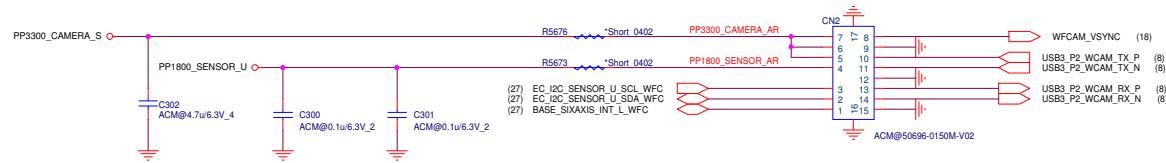
SELECT PER SEL SI TEAM
CM TO ADJUST PINOUT/PIN COUNT

- (8) USB3_P4_C1_TX_P
- (8) USB3_P4_C1_TX_N
- (8) USB2_P3_A1_N
- (8) USB2_P3_A1_P
- (8) USB3_P4_C1_RX_P
- (8) USB3_P4_C1_RX_N
- (8) USB2_P4_C1_P
- (8) USB2_P4_C1_N
- (7) DDH1_TX0_P
- (7) DDH1_TX0_N
- (7) DDH1_TX1_P
- (7) DDH1_TX1_N
- (7) DDH1_TX2_P
- (7) DDH1_TX2_N
- (7) DDH1_TX3_P
- (7) DDH1_TX3_N
- (8) USB3_P3_A1_RX_N
- (8) USB3_P3_A1_RX_P

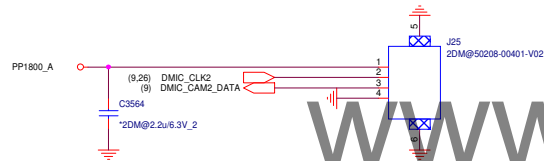
SELECT PER SEL SI TEAM

MOTHER BOARD INTERFACE

AR CAMERA CONN (ACM)



DMIC CONN (MIC2)



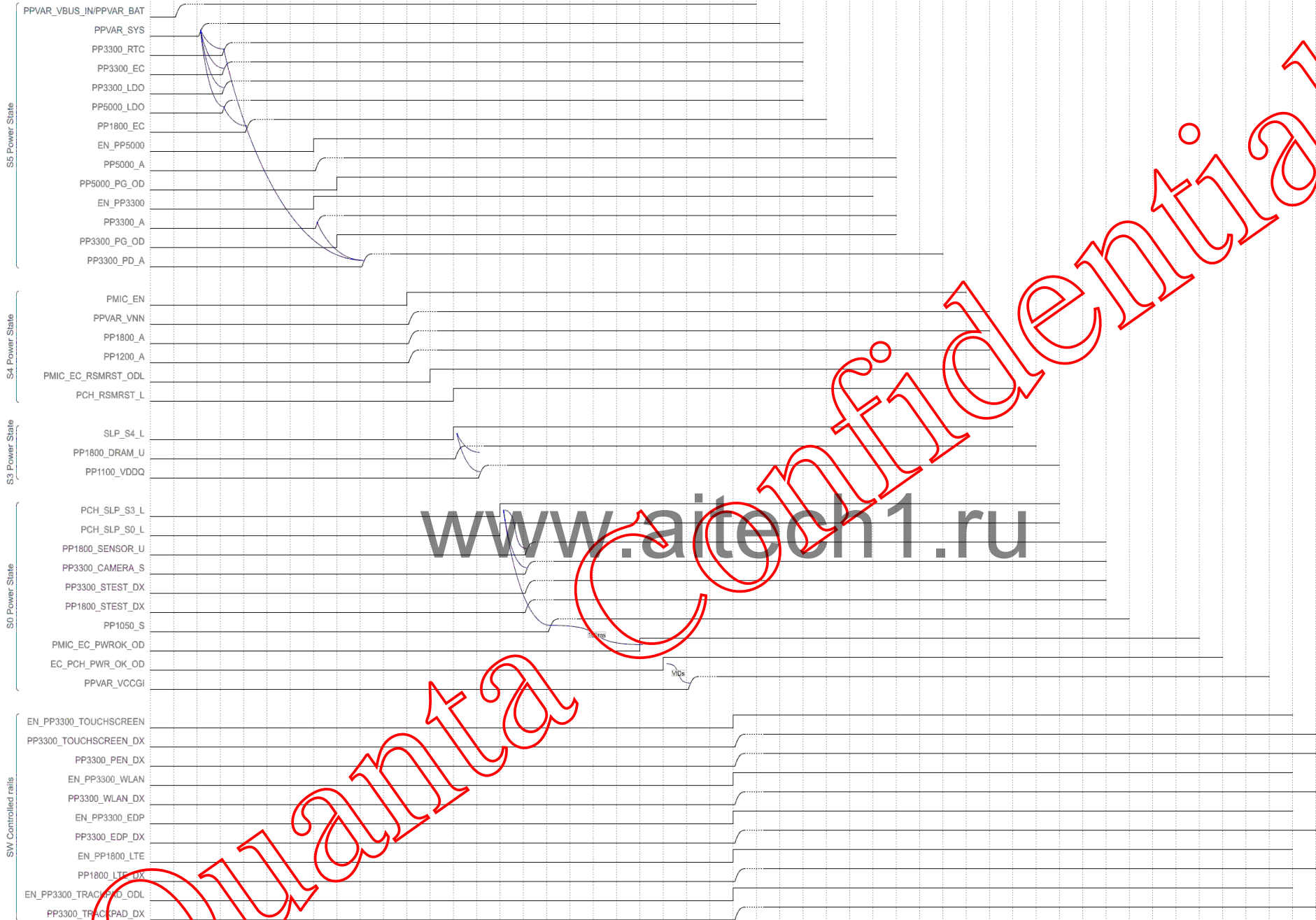
PREFERRED DMIC CHANNEL CONFIG
INTERFACE 1: STRAP MIC TO LEFT=CHANNEL 0
INTERFACE 2: STRAP MIC TO RIGHT=CHANNEL 3

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Quanta Confidential

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GPIO #	Bump Name	Voltage	Bootstrap Termination	Default Termination	Bootstrap Purpose	Bootstrap Usage	Bootstrap	Octopus Signal Name
GPIO_27	GPIO_27	1.8V	20K PU	20K PD	eMMC as boot Source 20K PU internal	1 = enable (default) 0 = disable	eMMC Boot	DBG_PTI_DATA_26
GPIO_28	GPIO_28	1.8V	20K PU	20K PD	SPI as boot Source 20K PU internal	1 = enable (default) 0 = disable	SPI Boot	DBG_PTI_DATA_27
GPIO_42	GP_INTD_DS1_TE1	1.8V	20K PD	20K PD	Flash Descriptor Override for SPI security features	1 = Override 0 = No Override (default)	Flash Descriptor	TP_WIFI_RST_N_TP135
GPIO_43	GP_INTD_DS1_TE2	1.8V	20K PU	20K PD	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GP_INTD_DS1_TE2
GPIO_44	USB_OC0_B	1.8V	20K PD	20K PU	RVSD	1 = Do Not Use 0 = disable (default)	RSVD	USB_A_OC_ODL
GPIO_45	USB_OC1_B	1.8V	20K PD	20K PU	Top Swap Override. Have core look for BIOS code in SPI ROM	1 = Enable 0 = disable (default)	Top Swap	USB_C_OC_ODL
GPIO_61	LPSS_UART0_TXD	1.8V	20K PD	20K PU	TXE to bypass ROM in SoC and go to patch space	1 = enable bypass 0 = disable (default)	TXE ROM Bypass	PCHTX_MIPSRX_UART
GPIO_62	LPSS_UART0_RTS	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_INT_L
GPIO_65	LPSS_UART2_TXD	1.8V	20K PD	20K PU	TXE to perform DnX for new FW Image over USB.	1 = Force DnX 0 = Do Not Force (default)	DoX FW Load	PCHTX_UART2
GPIO_66	LPSS_UART2_RTS	1.8V	20K PD	20K PU	LPC Boot BIOS strap	1 = LPC Boot 0 = No LPC Boot (default)	LPC Boot	LTE_OFF_ODL
GPIO_79	LPSS_SPI_0_CLK	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	H1_SLAVE_SPI_CLK_R
GPIO_80	LPSS_SPI_0_FSD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = No Halt (default)	RSVD	H1_SLAVE_SPI_CS_L_R
GPIO_81	LPSS_SPI_0_FS1	1.8V	20K PU	20K PU	RSVD	1 = Disable (default) 0 = Do Not Use	RSVD	GPIO_81_DEBUG (Boot halt)
GPIO_83	LPSS_SPI_0_TXD	1.8V	20K PD	20K PD	Sets the LPC buffer to 1.8V or 3.3V mode	1 = 1.8V mode 0 = 3.3V mode (default)	LPC Voltage Select	H1_SLAVE_SPI_MOSI_R
GPIO_84	LPSS_SPI_2_CLK	1.8V	20K PU	20K PD	SPI Boot BIOS Strap	1 = Do Not SPI Boot (default) 0 = SPI Boot. Debug if Secure boot fuse is set to 0	SPI Boot Source	stest_SPI1_CLK_R
GPIO_85	LPSS_SPI_2_FSD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = disable (default)	RSVD	stest_SPI_CS_L_R
GPIO_86	LPSS_SPI_2_FS1	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = enable (default)	RSVD	stest_CNTRL
GPIO_87	LPSS_SPI_2_FS2	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	TP_PCH_GPIO_87_PD
GPIO_89	LPSS_SPI_2_TXD	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	stest_SPI1_MOSI_R
GPIO_159	AVS_I2S0_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	I2S0_PCH_RX
GPIO_163	AVS_I2S1_WS_SYN	1.8V	20K PD	20K PD	SMBus 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	Buffers 1.8V/3.3V	I2S_SFRM_5PKR
GPIO_164	AVS_I2S1_SDI	1.8V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	WLAN_PE_RST
GPIO_168	AVS_HDA_SDI	1.8V	20K PD	20K PD	PMU 3.3V/1.8V mode select	1 = 1.8V mode 0 = 3.3V mode (default)	PMU 1.8V/3.3V	I2S2_PCH_RX
GPIO_172	AVS_M_CLK_B1	1.8V	20K PD	20K PD	SMBus No Reboot. Handled by PMC	1 = Enable 0 = disable (default)	SMBus Reboot	DMIC_CLK2_R
GPIO_174	AVS_M_CLK_AB2	1.8V	20K PD	20K PD	VDD2 Voltage Select	1 = 1.24V 0 = 1.20V (default)	VDD2 Voltage	(Open, TP_GPIO_174)
GPIO_175	AVS_M_DATA_2	1.8V	20K PD	20K PD	eSPI vs. LPC	1 = eSPI mode 0 = LPC mode (default)	eSPI/LPC mode	DMIC_CAM2_DATA
GPIO_177	SMB_CLK	1.8V/3.3V	20K PD	20K PD	RSVD	1 = Do Not Use 0 = Default	RSVD	(Open, TP160)
GPIO_191	CNV_BRI_DT	1.8V	20K PD	None	eSPI Flash Sharing Mode. Set to 0 if GPIO_175 is set to 0	1 = Slave attached Share 0 = Master attached (default)	Flash Sharing	CNVI_BRI_DT_R
GPIO_192	CNV_BRI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_BRI_RSP
GPIO_193	CNV_RFI_DT	1.8V	20K PU	None	RSVD	1 = Normal Operation 0 = Do not use	RSVD	CNVI_RFI_DT_R
GPIO_194	CNV_RFI_RSP	1.8V	20K PD	20K PU	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_RFI_RSP
GPIO_195	CNV_RF_RESET_L	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	CNVI_RF_RESET_L
GPIO_196	XTAL_CLKREQ	1.8V	20K PD	None	RSVD	1 = Do Not Use 0 = Normal Operation	RSVD	(Not available)